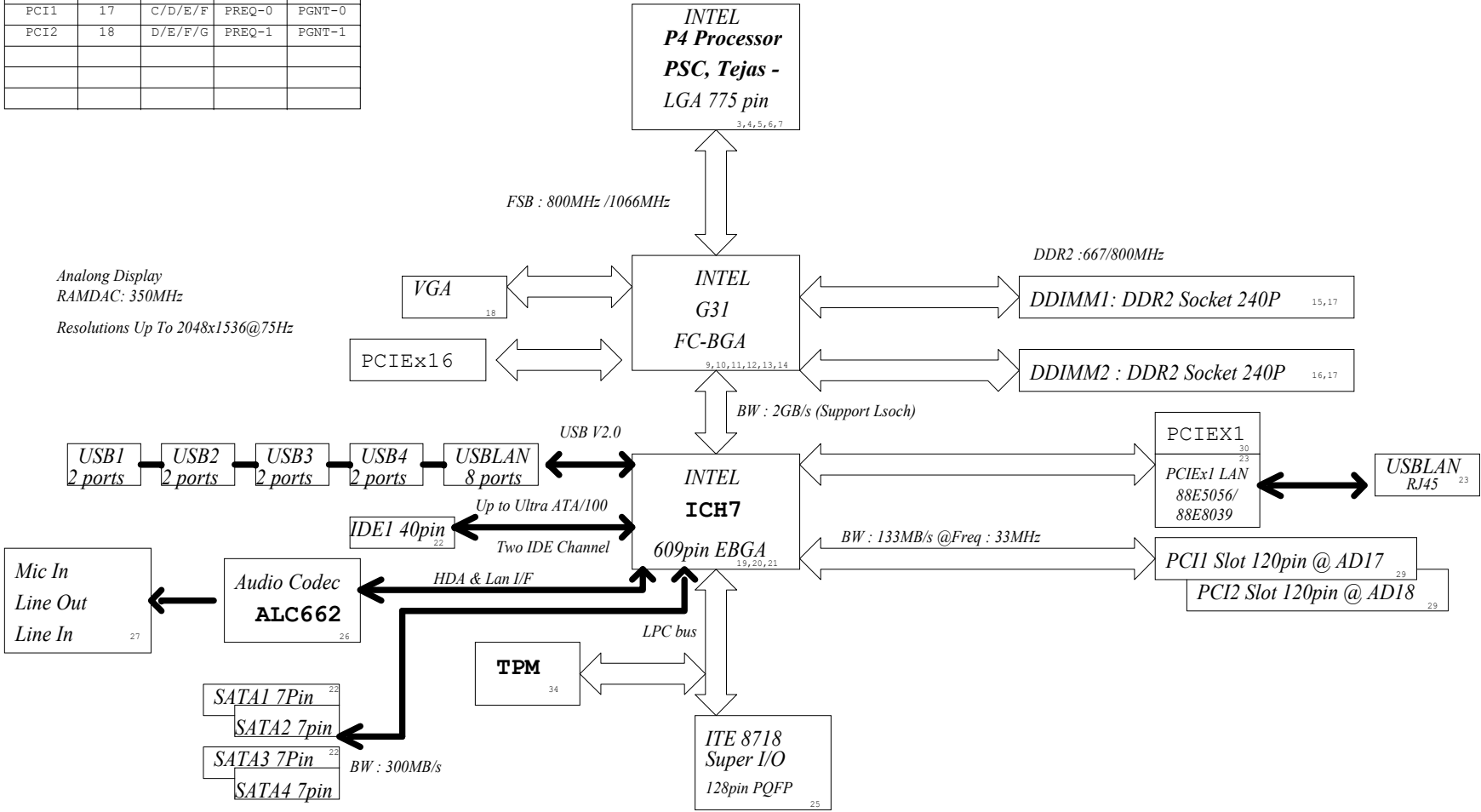


G31T-LM Rev: 1.0

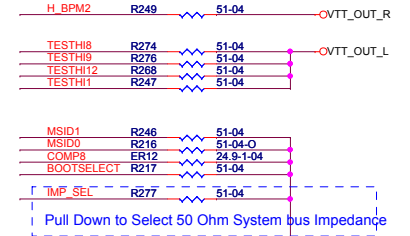
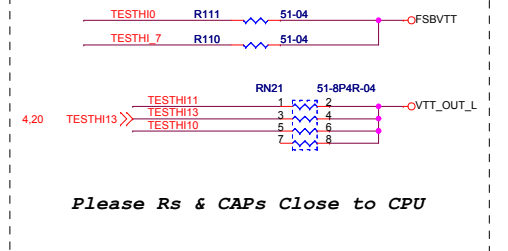
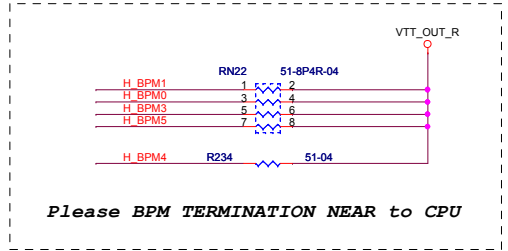
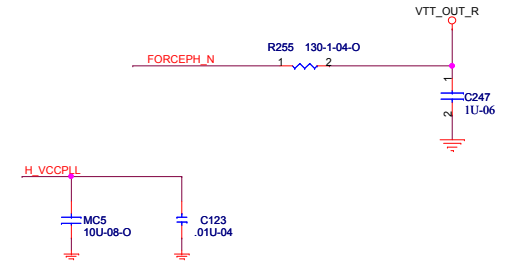
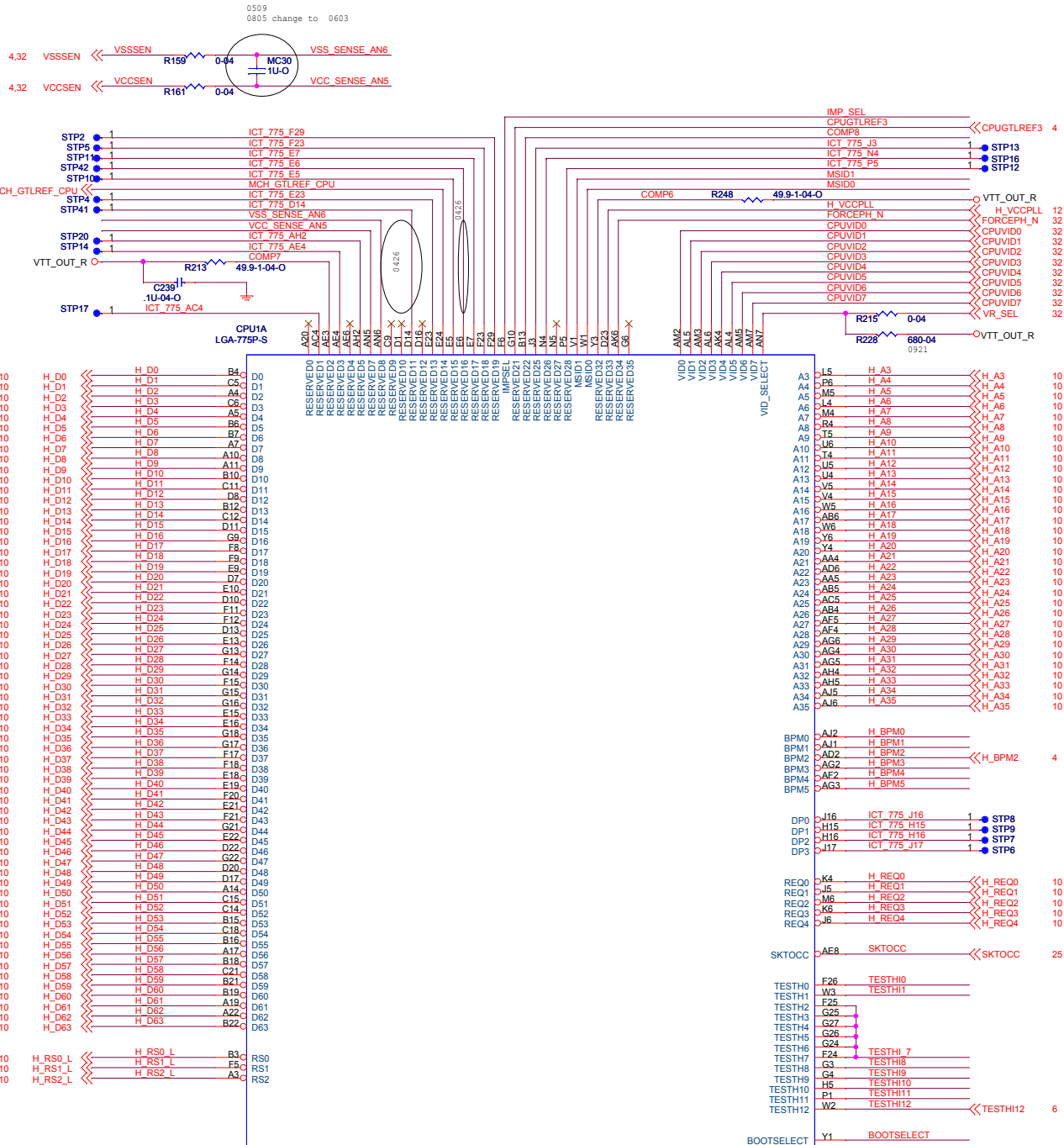
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DEVICE	IDSEL	INT#	REQ#	GNT#
PCI1	17	C/D/E/F	PREQ-0	PGNT-0
PCI2	18	D/E/F/G	PREQ-1	PGNT-1

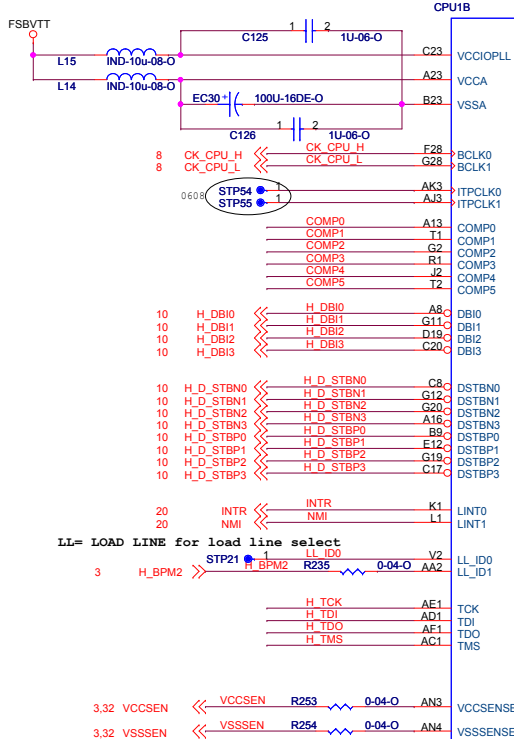


PCB : 244 x 244 mm ; 4 layers

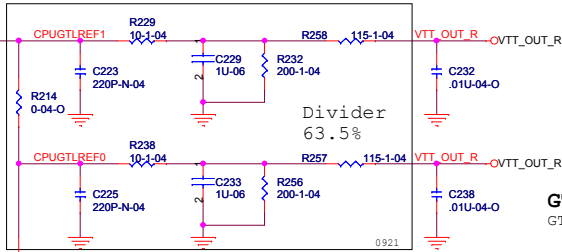


	2005B(130W) Performance FMB	2005B(95W) Mainstream FMB
MSID1	pull-down	pull-down
MSID0	pull-down	NC

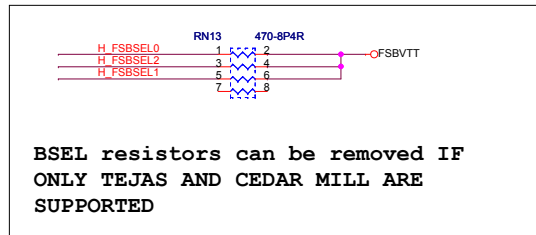
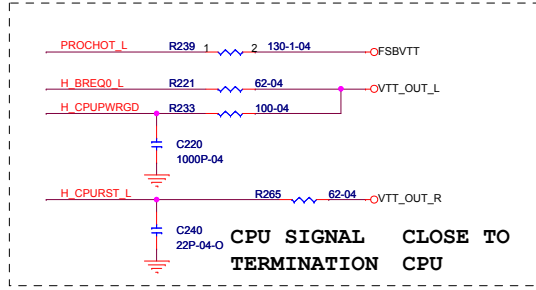
Place componets as close as possible to Processor socket
trace width to cap must be no smaller than 12 Mils



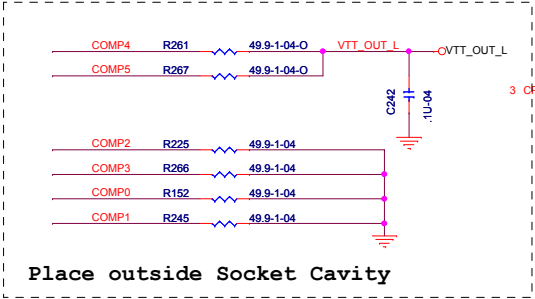
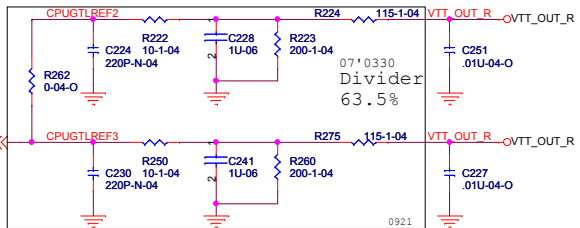
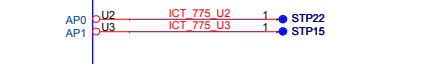
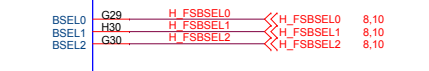
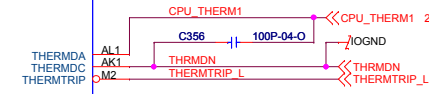
LGA-775P-S



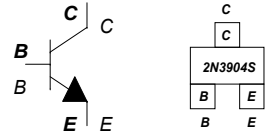
$GTLREF = 0.67 * VTT = 0.8V$
GTLREF GENERATION CIRCUITS



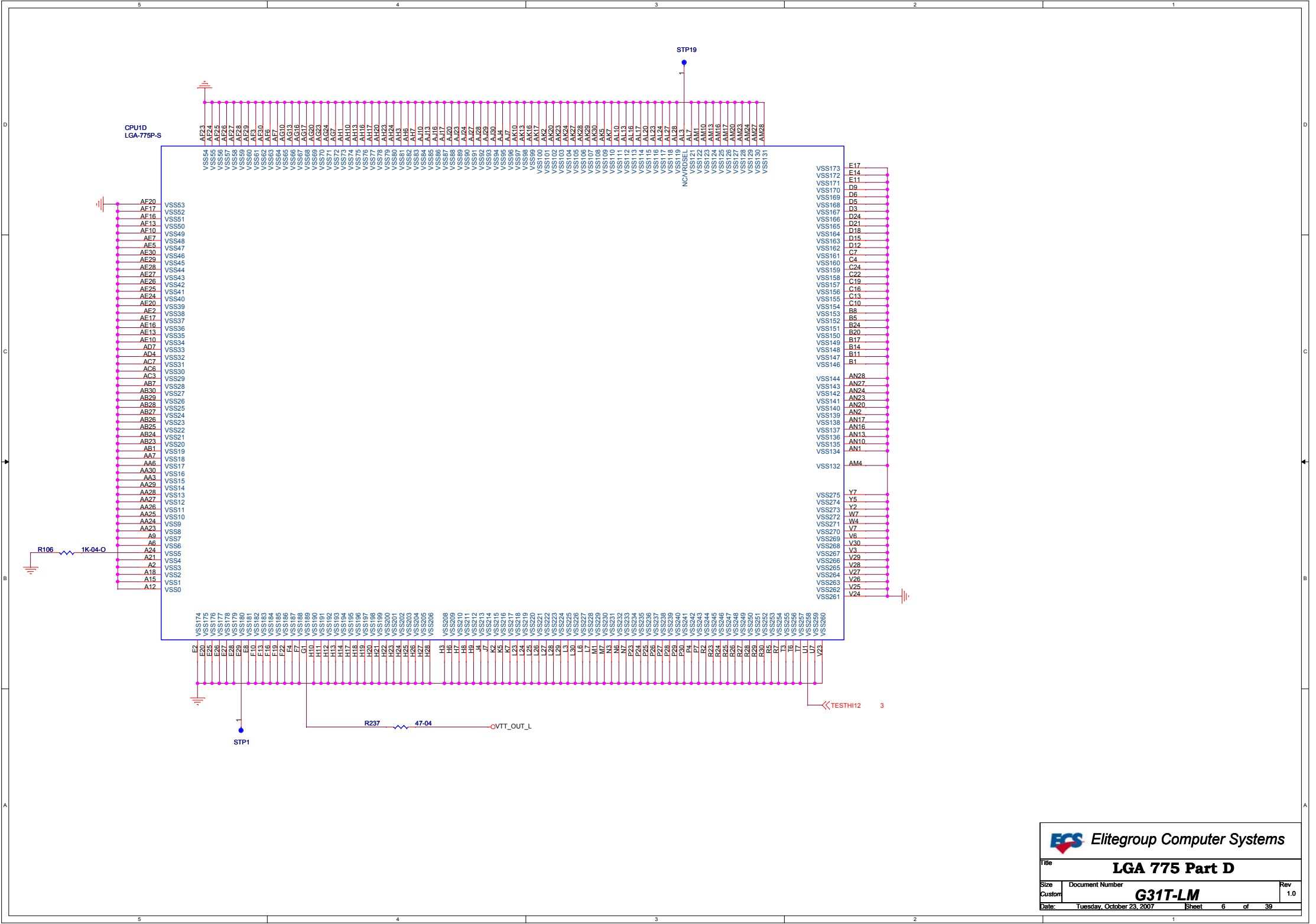
GPIO	A20M	K3	A20M_L	<<A20M_L	20
	ADS	D2	H ADS_L	<<ADS_L	10
	ADSTB0	R6	H A_STB0	<<H_A_STB0	10
	ADSTB1	AD5	H A_STB1	<<H_A_STB1	10
	BNIT	AD3	ICT 775 AD3		1
	BNR	G8	H BNR_L	<<H_BNR_L	10
	BPRI	C2	H BPRI_L	<<BPRI_L	10
	BR0	G2	H BRE0_L	<<H_BRE0_L	10
	DBR	AC2	H HWBST_L	<<H_HWBST_L	8,19,28
	DBSY	F2	H DBSY_L	<<H_DBSY_L	10
	DEFER	G7	H DEFER_L	<<H_DEFER_L	10
	DRDY	C1	H DRDY_L	<<H_DRDY_L	10
	EDRDY	F2	CPUGTREF2		10
	FERRPBE	R3	FERR_L	<<FERR_L	20
	HIT	D4	H HIT_L	<<H_HIT_L	20
	HITM	E4	H HITM_L	<<H_HITM_L	10
	IERR	AB2	H IERR_L	<<H_IERR_L	10
	IGNNE	N2	IGNNE_L	<<IGNNE_L	20
	INIT	P3	HINIT_L		10
	LOCK	C3	H LOCK_L	<<H_LOCK_L	10
	MCERR	AB3	X		
	PC REQ	AL2	X	<<PECI	25
	PROCHOT	G5	PROCHOT_L	<<PROCHOT_L	32
	PWRGOOD	N1	H CPUPWRGD	<<H_CPUPWRGD	19
	RESET	G23	H CPURST_L	<<H_CPURST_L	10
	RSP	L2	TESTH13		3,20
SLP	P2	SMI_L	<<TESTH13	19,20	
SMI	M3	STPCLK_L	<<SMI_L	20	
STPCLK	AG1	H TRDY_L	<<H_STPCLK_L	20	
TRDY	M3	H TRDY_L	<<H_TRDY_L	10	
TRST	AG1	H TRST_L		10	

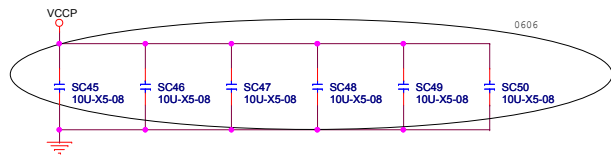


Place outside Socket Cavity

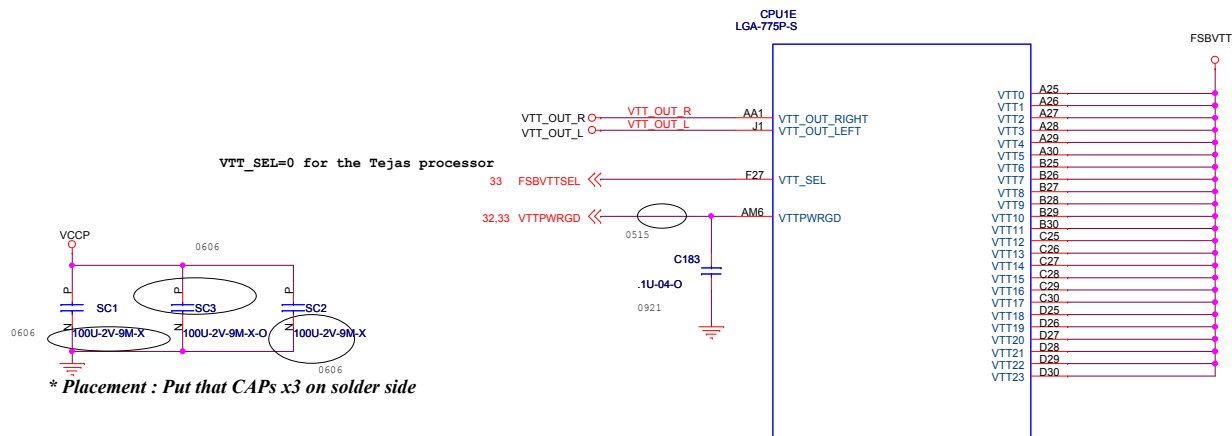
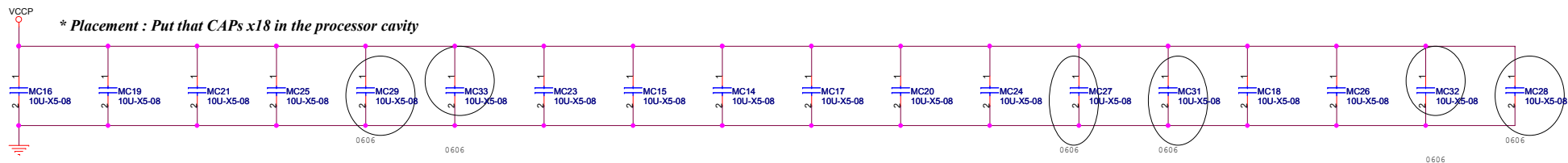


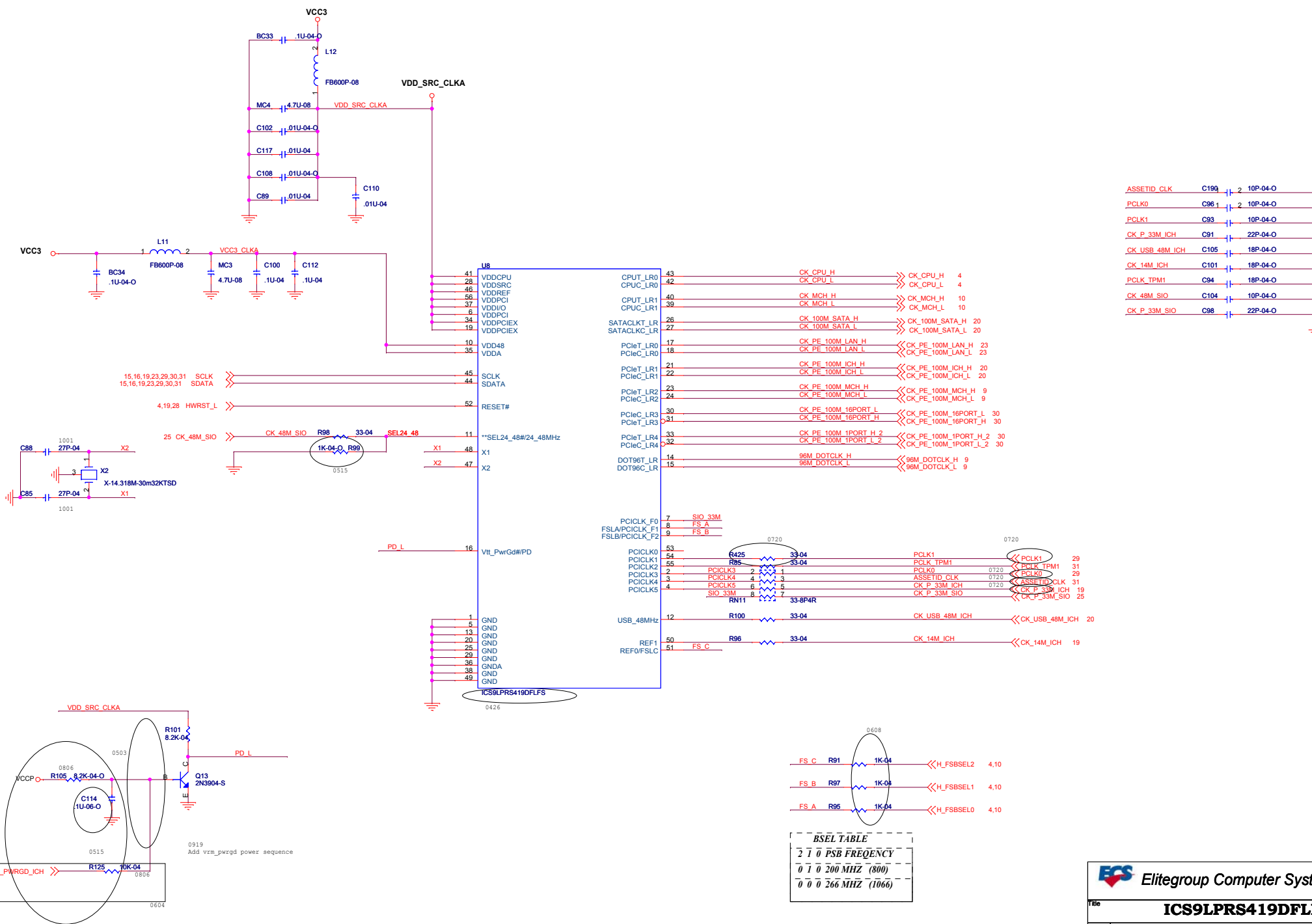






070117_change






ASSETID_CLK	C190	2	10P-04-O
PCLK0	C96	1	2 10P-04-O
PCLK1	C93		10P-04-O
CK_P_33M_ICH	C91		22P-04-O
CK_USB_48M_ICH	C105		18P-04-O
CK_14M_ICH	C101		18P-04-O
PCLK_TPM1	C94		18P-04-O
CK_48M_SIO	C104		10P-04-O
CK_P_33M_SIO	C98		22P-04-O

PCICLK_F0	7	SIO_33M
FSLA/PCICLK_F1	8	FS_A
FSLB/PCICLK_F2	9	FS_B

PCICLK0	53	
PCICLK1	54	
PCICLK2	55	
PCICLK3	2	
PCICLK4	4	
PCICLK5	6	
SIO_33M	8	

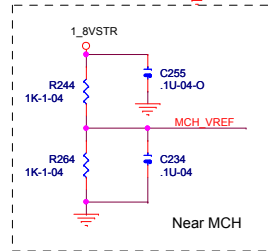
FS_C	R91	1K-04	H_FSBSEL2	4,10
FS_B	R97	1K-04	H_FSBSEL1	4,10
FS_A	R95	1K-04	H_FSBSEL0	4,10

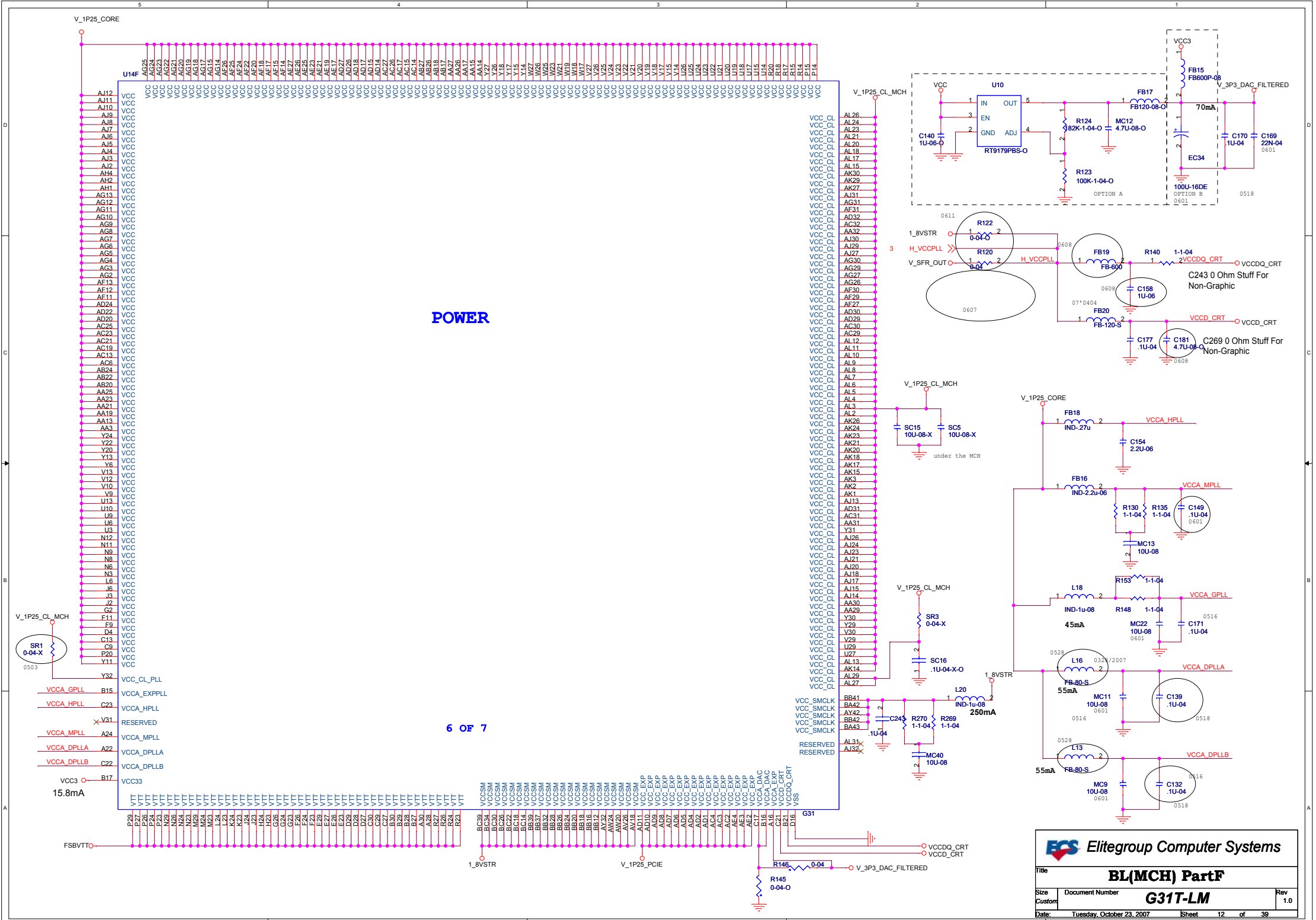
BSEL TABLE	
2	1 0 PSB FREQUENCY
0	1 0 200 MHz (800)
0	0 0 266 MHz (1066)

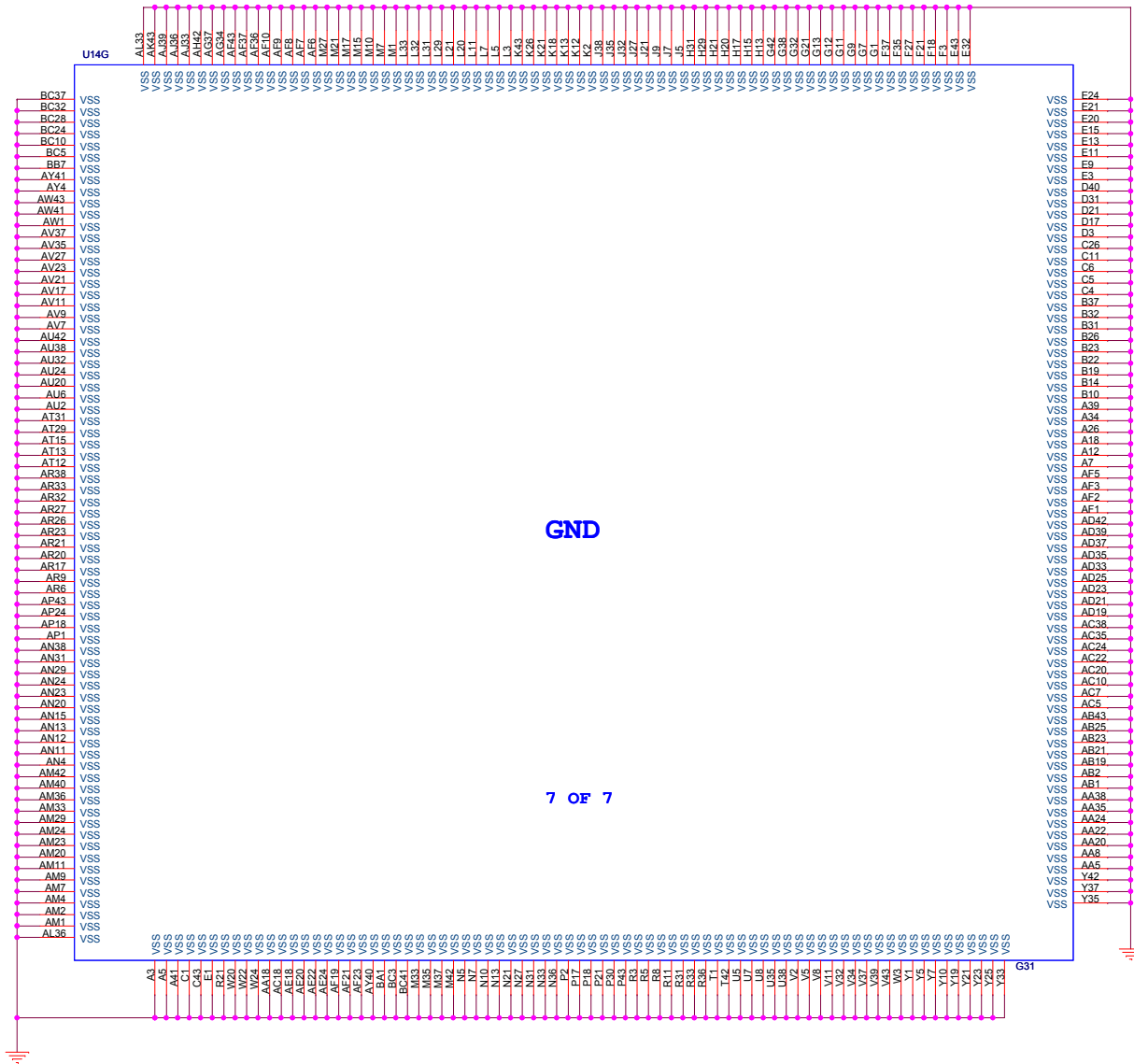
**Elitegroup Computer Systems**

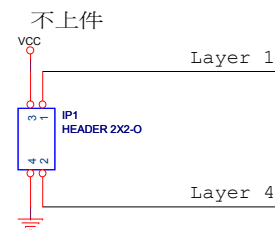
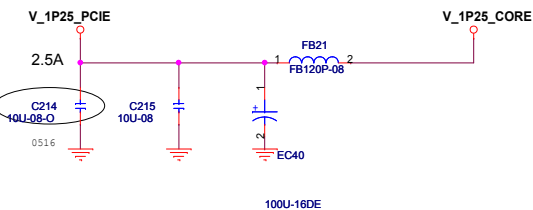
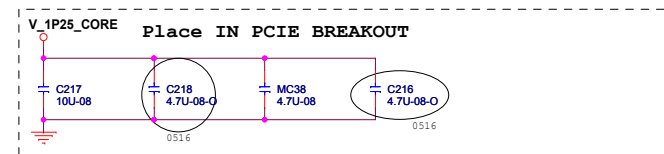
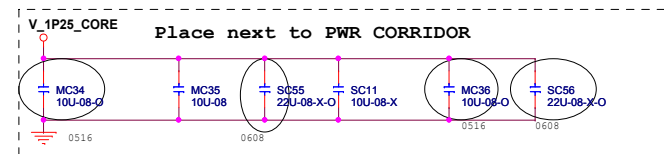
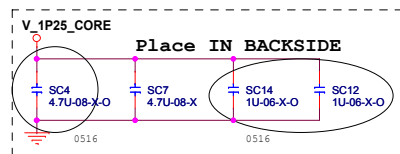
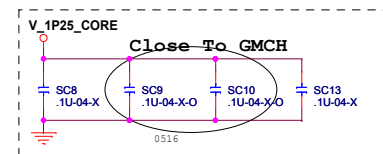
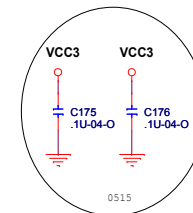
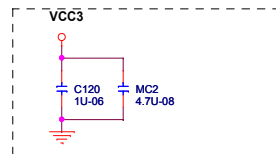
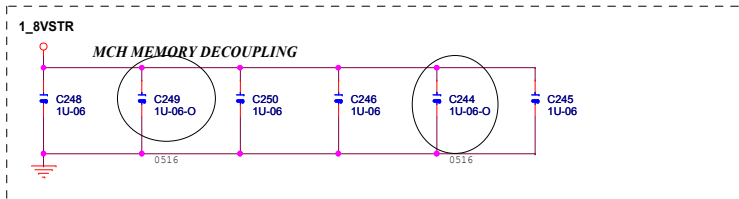
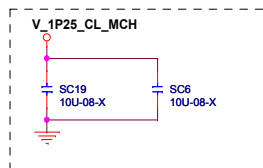
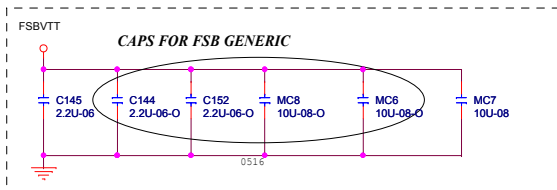
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Size	Document Number	Rev			
Custom	G31T-LM			1.0	
Date:	Tuesday, October 23, 2007			Sheet	8 of 39

U14B 01MCH									
3	H_D0	H_D0	R40	HD0	HA#3	J42	H_A3	H_A3	3
3	H_D1	H_D1	P41	HD1	HA#4	L39	H_A4	H_A4	3
3	H_D2	H_D2	R41	HD2	HA#5	L40	H_A5	H_A5	3
3	H_D3	H_D3	N40	HD3	HA#6	L37	H_A6	H_A6	3
3	H_D4	H_D4	R42	HD4	HA#7	L36	H_A7	H_A7	3
3	H_D5	H_D5	M39	HD5	HA#8	N32	H_A8	H_A8	3
3	H_D6	H_D6	N41	HD6	HA#9	N32	H_A9	H_A9	3
3	H_D7	H_D7	N42	HD7	HA#10	N34	H_A10	H_A10	3
3	H_D8	H_D8	L41	HD8	HA#11	M38	H_A11	H_A11	3
3	H_D9	H_D9	L42	HD9	HA#12	M37	H_A12	H_A12	3
3	H_D10	H_D10	J41	HD10	HA#13	M36	H_A13	H_A13	3
3	H_D11	H_D11	K41	HD11	HA#14	R34	H_A14	H_A14	3
3	H_D12	H_D12	G40	HD12	HA#15	N35	H_A15	H_A15	3
3	H_D13	H_D13	F41	HD13	HA#16	N38	H_A16	H_A16	3
3	H_D14	H_D14	F42	HD14	HA#17	N37	H_A17	H_A17	3
3	H_D15	H_D15	C42	HD15	HA#18	N39	H_A18	H_A18	3
3	H_D16	H_D16	D41	HD16	HA#19	R37	H_A19	H_A19	3
3	H_D17	H_D17	F38	HD17	HA#20	F42	H_A20	H_A20	3
3	H_D18	H_D18	G37	HD18	HA#21	V36	H_A21	H_A21	3
3	H_D19	H_D19	F39	HD19	HA#22	V36	H_A22	H_A22	3
3	H_D20	H_D20	E42	HD20	HA#23	R38	H_A23	H_A23	3
3	H_D21	H_D21	E39	HD21	HA#24	U36	H_A24	H_A24	3
3	H_D22	H_D22	E37	HD22	HA#25	U33	H_A25	H_A25	3
3	H_D23	H_D23	C39	HD23	HA#26	R35	H_A26	H_A26	3
3	H_D24	H_D24	B39	HD24	HA#27	V33	H_A27	H_A27	3
3	H_D25	H_D25	G33	HD25	HA#28	V35	H_A28	H_A28	3
3	H_D26	H_D26	F33	HD26	HA#29	V42	H_A29	H_A29	3
3	H_D27	H_D27	E35	HD27	HA#30	V38	H_A30	H_A30	3
3	H_D28	H_D28	K32	HD28	HA#31	Y36	H_A31	H_A31	3
3	H_D29	H_D29	H32	HD29	HA#32	Y36	H_A32	H_A32	3
3	H_D30	H_D30	B34	HD30	HA#33	Y38	H_A33	H_A33	3
3	H_D31	H_D31	J31	HD31	HA#34	Y39	H_A34	H_A34	3
3	H_D32	H_D32	F32	HD32	HA#35	AA37	H_A35	H_A35	3
3	H_D33	H_D33	M31	HD33	HREQ0#	F40	H_REQ0	H_REQ0	3
3	H_D34	H_D34	E35	HD34	HREQ1#	C35	H_REQ1	H_REQ1	3
3	H_D35	H_D35	K31	HD35	HREQ2#	L38	H_REQ2	H_REQ2	3
3	H_D36	H_D36	G31	HD36	HREQ3#	G43	H_REQ3	H_REQ3	3
3	H_D37	H_D37	K29	HD37	HREQ4#	J37	H_REQ4	H_REQ4	3
3	H_D38	H_D38	F31	HD38	HREQ0#	M34	H_A_STB0	H_A_STB0	4
3	H_D39	H_D39	J29	HD39	HREQ1#	U34	H_A_STB1	H_A_STB1	4
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3	H_D42	H_D42	K27	HD42	HREQ4#	M40	H_D_STBN1	H_D_STBN1	4
3	H_D43	H_D43	H26	HD43	HREQ0#	G35	H_D_STBP1	H_D_STBP1	4
3	H_D44	H_D44	L26	HD44	HREQ1#	H33	H_D_STBN1	H_D_STBN1	4
3	H_D45	H_D45	J26	HD45	HREQ2#	C33	H_D_STBP2	H_D_STBP2	4
3	H_D46	H_D46	M26	HD46	HREQ3#	H27	H_D_STBN2	H_D_STBN2	4
3	H_D47	H_D47	C33	HD47	HREQ4#	G29	H_D_STBP3	H_D_STBP3	4
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3	H_D49	H_D49	E41	HD49	HREQ1#	D38	H_D_STBN3	H_D_STBN3	4
3	H_D50	H_D50	B41	HD50	HREQ2#	E33	H_DBI3	H_DBI3	4
3	H_D51	H_D51	D42	HD51	HREQ3#	W40	H_ADS_L	H_ADS_L	4
3	H_D52	H_D52	C40	HD52	HREQ4#	Y40	H_TRDY_L	H_TRDY_L	4
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3	H_D55	H_D55	D37	HD55	HREQ2#	Y43	H_HITM_L	H_HITM_L	4
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3	H_D61	H_D61	B32	HD61	HREQ3#	U40	H_DBSY_L	H_DBSY_L	4
3	H_D62	H_D62	A32	HD62	HREQ4#	U41	H_RS0_L	H_RS0_L	3
3	H_D63	H_D63	B32	HD63	HREQ0#	AA41	H_RS1_L	H_RS1_L	3
3	H_D64	H_D64	A32	HD64	HREQ1#	U39	H_RS2_L	H_RS2_L	3
3	H_D65	H_D65	B32	HD65	HREQ2#	G31	H_CPURST_L	H_CPURST_L	4
3	H_D66	H_D66	A32	HD66	HREQ3#				
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3	H_D68	H_D68	A32	HD68	HREQ0#				
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3	H_D75	H_D75	B32	HD75	HREQ2#				
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3	H_D92	H_D92	A32	HD92	HREQ4#				
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3	H_D97	H_D97	B32	HD97	HREQ4#				
3	H_D98	H_D98	A32	HD98	HREQ0#				
3	H_D99	H_D99	B32	HD99	HREQ1#				
3	H_D100	H_D100	A32	HD100	HREQ2#				
3	H_D101	H_D101	B32	HD101	HREQ3#				
3	H_D102	H_D102	A32	HD102	HREQ4#				
3	H_D103	H_D103	B32	HD103	HREQ0#				
3	H_D104	H_D104	A32	HD104	HREQ1#				
3	H_D105	H_D105	B32	HD105	HREQ2#				
3	H_D106	H_D106	A32	HD106	HREQ3#				
3	H_D107	H_D107	B32	HD107	HREQ4#				
3	H_D108	H_D108	A32	HD108	HREQ0#				
3	H_D109	H_D109	B32	HD109	HREQ1#				
3	H_D110	H_D110	A32	HD110	HREQ2#				
3	H_D111	H_D111	B32	HD111	HREQ3#				
3	H_D112	H_D112	A32	HD112	HREQ4#				
3	H_D113	H_D113	B32	HD113	HREQ0#				
3	H_D114	H_D114	A32	HD114	HREQ1#				
3	H_D115	H_D115	B32	HD115	HREQ2#				
3	H_D116	H_D116	A32	HD116	HREQ3#				
3	H_D117	H_D117	B32	HD117	HREQ4#				
3	H_D118	H_D118	A32	HD118	HREQ0#				
3	H_D119	H_D119	B32	HD119	HREQ1#				
3	H_D120	H_D120	A32	HD120	HREQ2#				
3	H_D121	H_D121	B32	HD121	HREQ3#				
3	H_D122	H_D122	A32	HD122	HREQ4#				
3	H_D123	H_D123	B32	HD123	HREQ0#				
3	H_D124	H_D124	A32	HD124	HREQ1#				
3	H_D125	H_D125	B32	HD125	HREQ2#				
3	H_D126	H_D126	A32	HD126	HREQ3#				
3	H_D127	H_D127	B32	HD127	HREQ4#				
3	H_D128	H_D128	A32	HD128	HREQ0#				
3	H_D129	H_D129	B32	HD129	HREQ1#				
3	H_D130	H_D130	A32	HD130	HREQ2#				
3	H_D131	H_D131	B32	HD131	HREQ3#				
3	H_D132	H_D132	A32	HD132	HREQ4#				
3	H_D133	H_D133	B32	HD133	HREQ0#				
3	H_D134	H_D134	A32	HD134	HREQ1#				
3	H_D135	H_D135	B32	HD135	HREQ2#				
3	H_D136	H_D136	A32	HD136	HREQ3#				
3	H_D137	H_D137	B32	HD137	HREQ4#				
3	H_D138	H_D138	A32	HD138	HREQ0#				
3	H_D139	H_D139	B32	HD139	HREQ1#				
3	H_D140	H_D140	A32	HD140	HREQ2#				
3	H_D141	H_D141	B32	HD141	HREQ3#				
3	H_D142	H_D142	A32	HD142	HREQ4#				
3	H_D143	H_D143	B32	HD143	HREQ0#				
3	H_D144	H_D144	A32	HD144	HREQ1#				
3	H_D145	H_D145	B32	HD145	HREQ2#				
3	H_D146	H_D146	A32	HD146	HREQ3#				
3	H_D147	H_D147	B32	HD147	HREQ4#				
3	H_D148	H_D148	A32	HD148	HREQ0#				
3	H_D149	H_D149	B32	HD149	HREQ1#				
3	H_D150	H_D150	A32	HD150	HREQ2#				
3	H_D151	H_D151	B32	HD151	HREQ3#				
3	H_D152	H_D152	A32	HD152	HREQ4#				
3	H_D153	H_D153	B32	HD153	HREQ0#				
3	H_D154	H_D154	A32	HD154	HREQ1#				
3	H_D155	H_D155	B32	HD155	HREQ2#				
3	H_D156	H_D156	A32	HD156	HREQ3#				
3	H_D157	H_D157	B32	HD157	HREQ4#				
3	H_D158	H_D158	A32	HD158	HREQ0#				
3	H_D159	H_D159	B32	HD159	HREQ1#				
3	H_D160	H_D160	A32	HD160	HREQ2#				
3	H_D161	H_D161	B32	HD161	HREQ3#				
3	H_D162	H_D162	A32	HD162	HREQ4#				
3	H_D163	H_D163	B32	HD163	HREQ0#				
3	H_D164	H_D164	A32	HD164	HREQ1#				
3	H_D165	H_D165	B32	HD165	HREQ2#				
3	H_D166	H_D166	A32	HD166	HREQ3#				



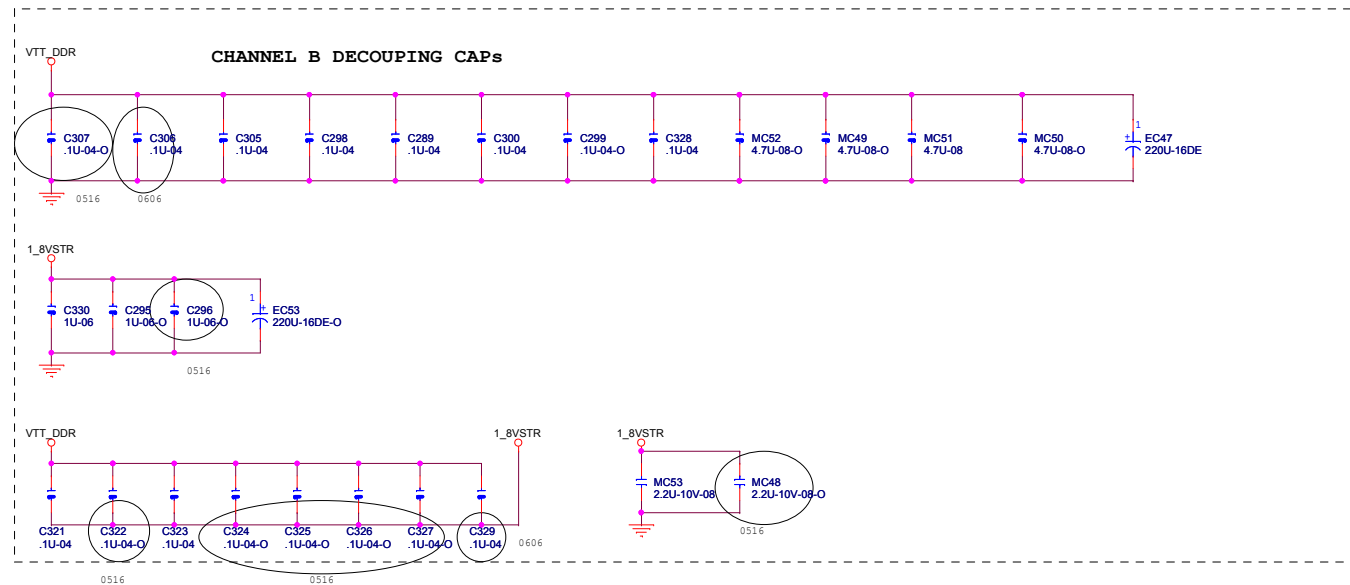
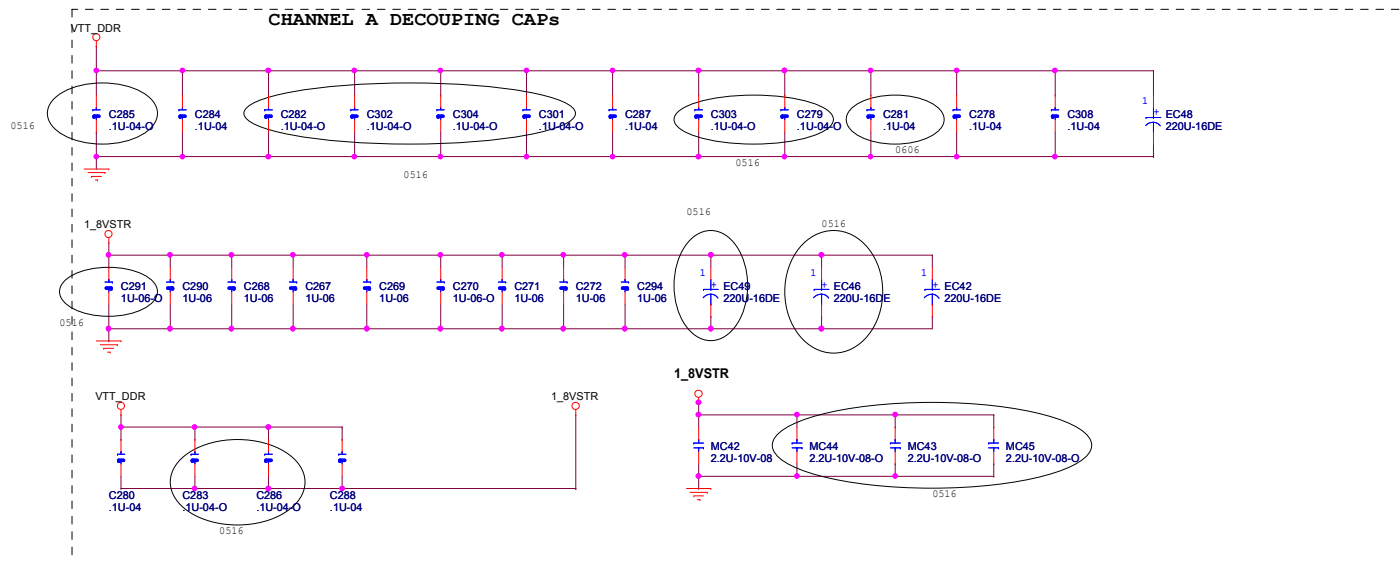


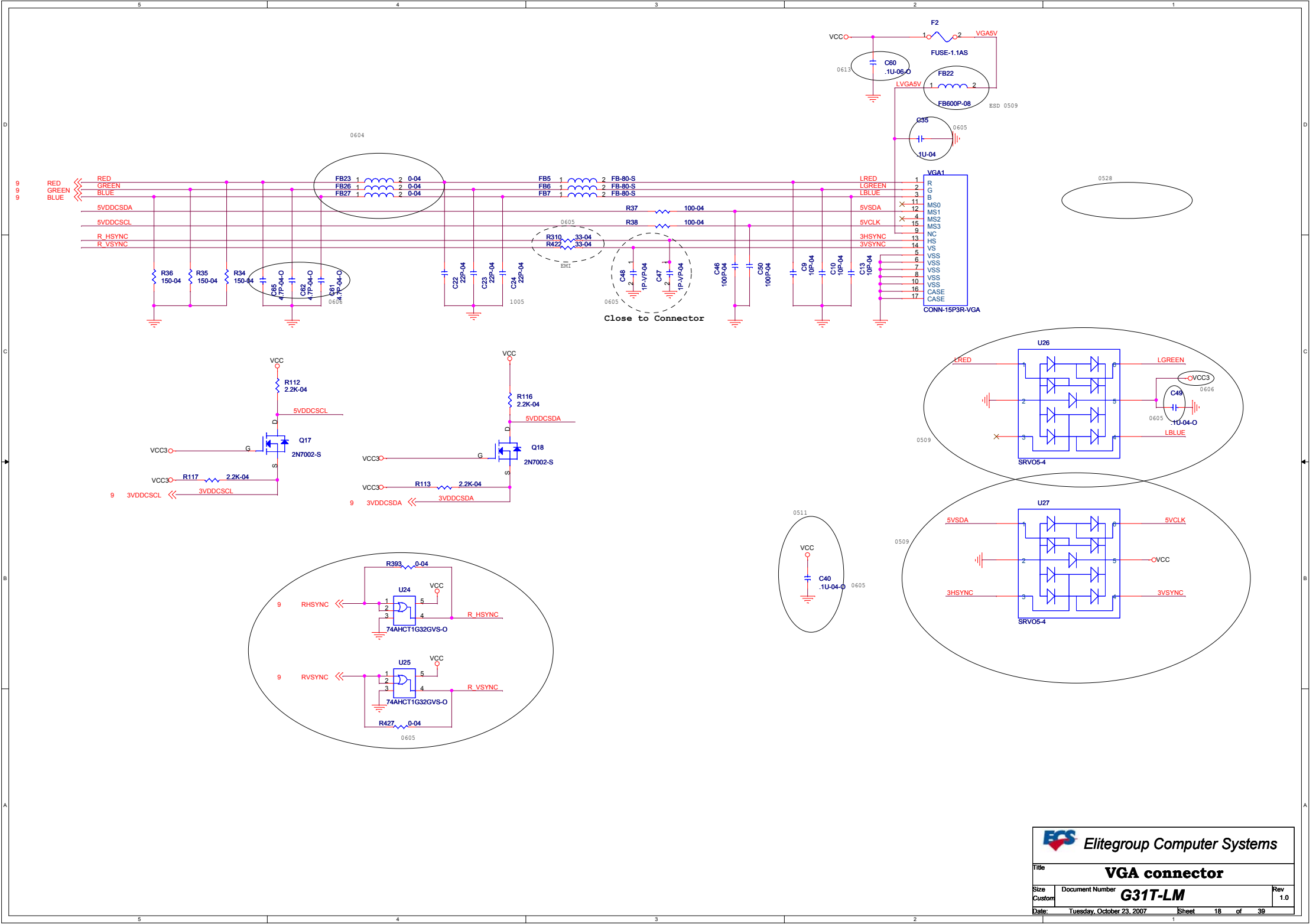


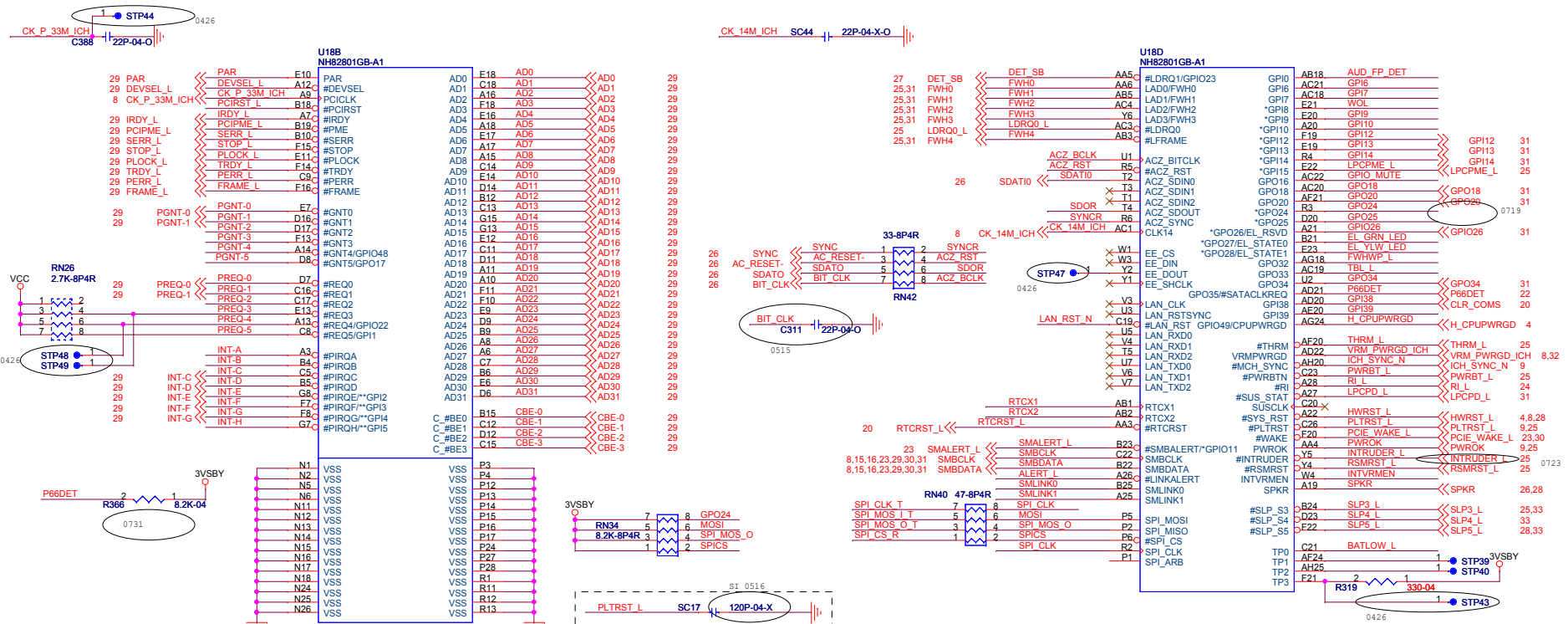


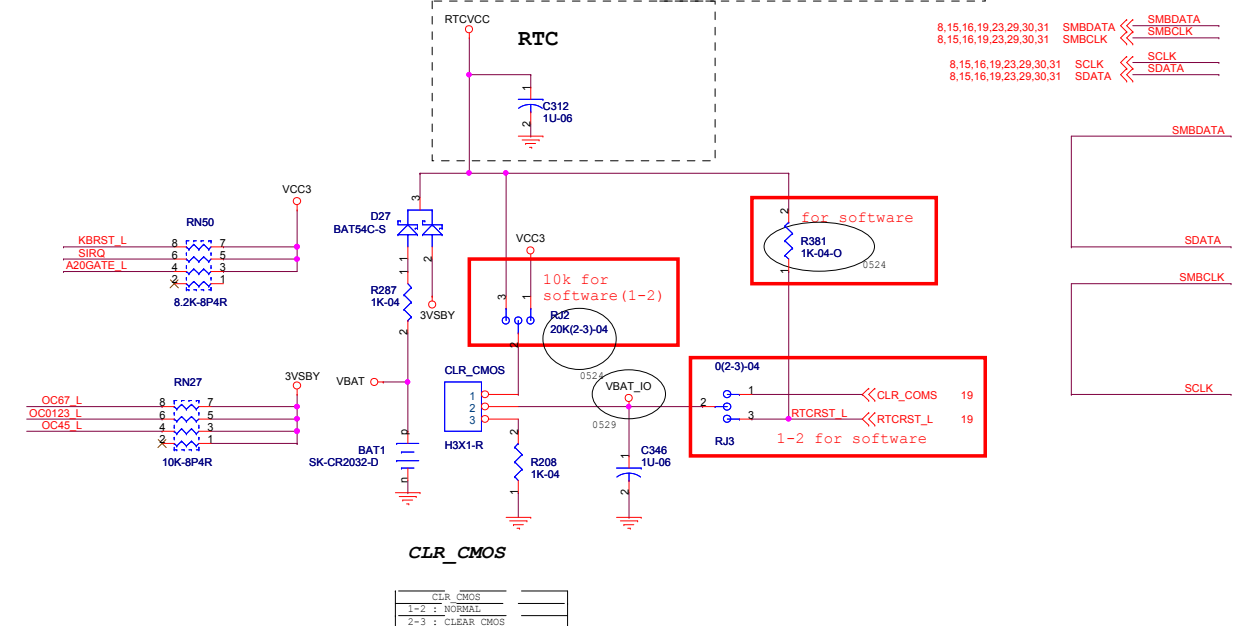
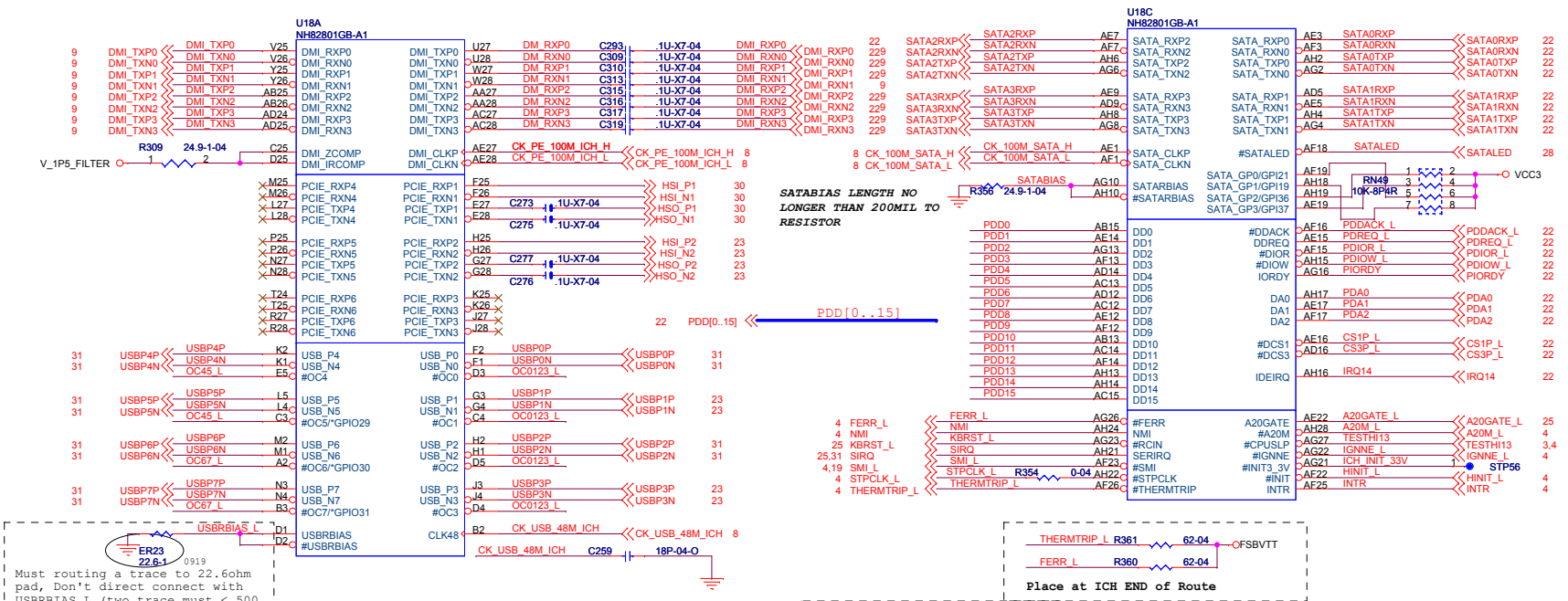
2116 : trace width 5 mil 60 ohm
Trace Length 3500 mils
Spacing: 1.clearance to itself 20/5/20(S:W:S)
2.clearance to other signal 3W

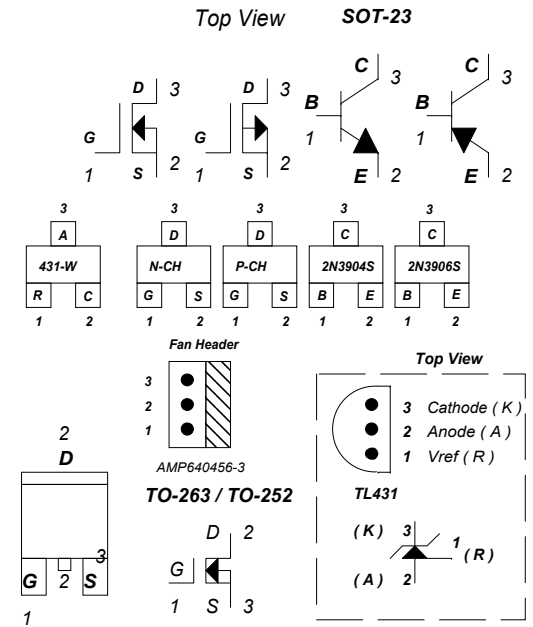
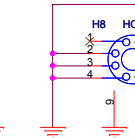
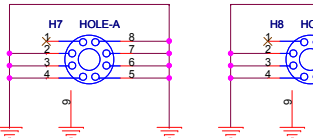
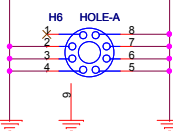
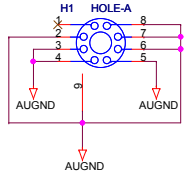
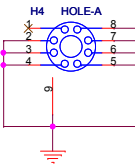
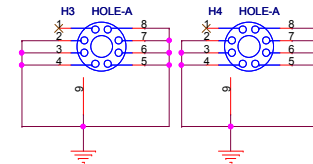
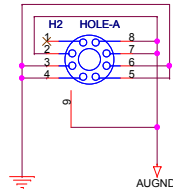
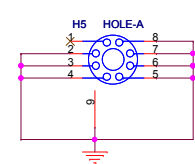
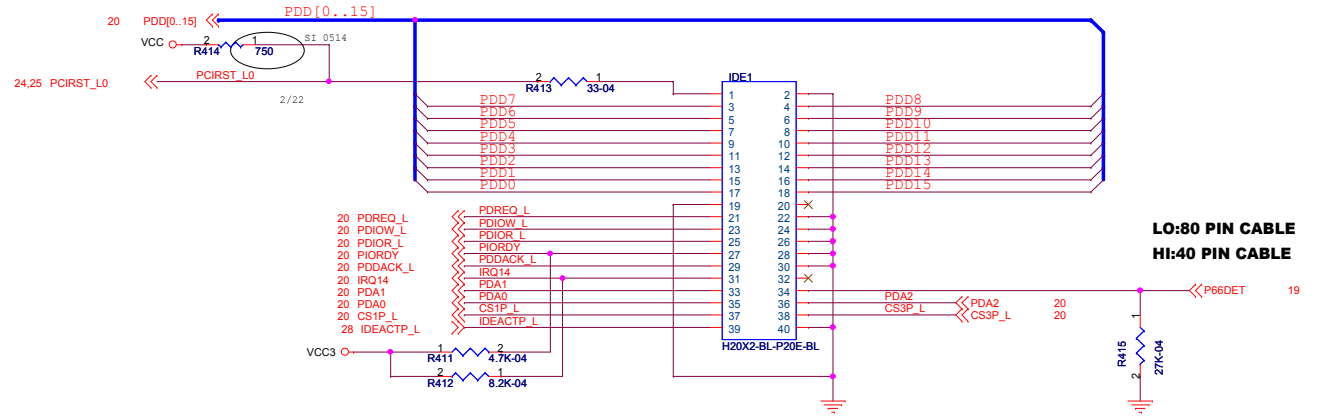
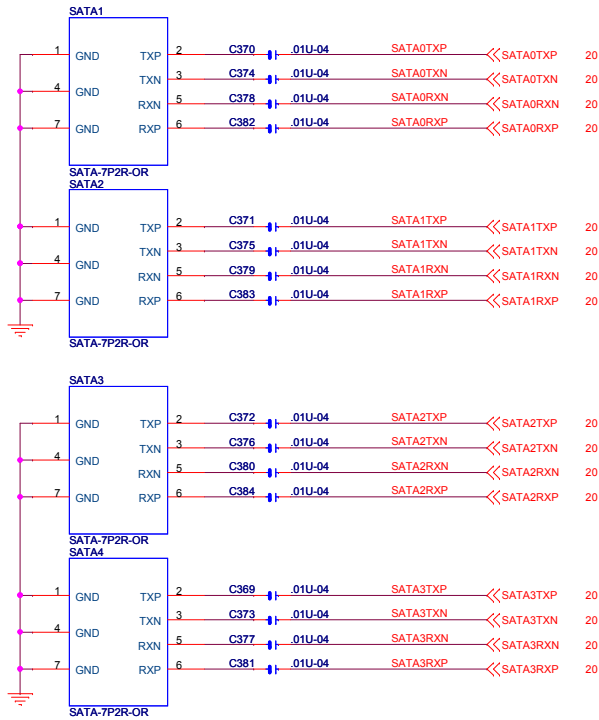
1080 : trace width 4 mil 50 ohm
Trace Length 3150 mils
Spacing: 1.clearance to itself 50/4/50(S:W:S)
2.clearance to other signal 3W

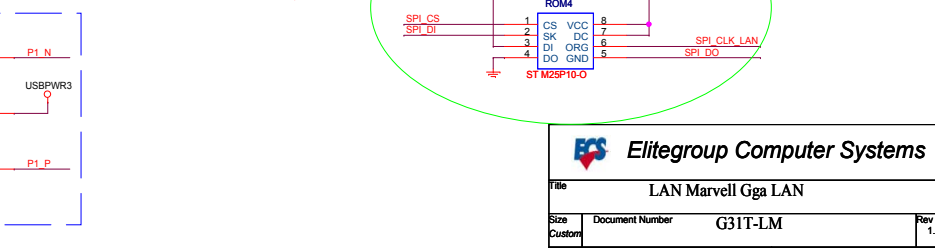
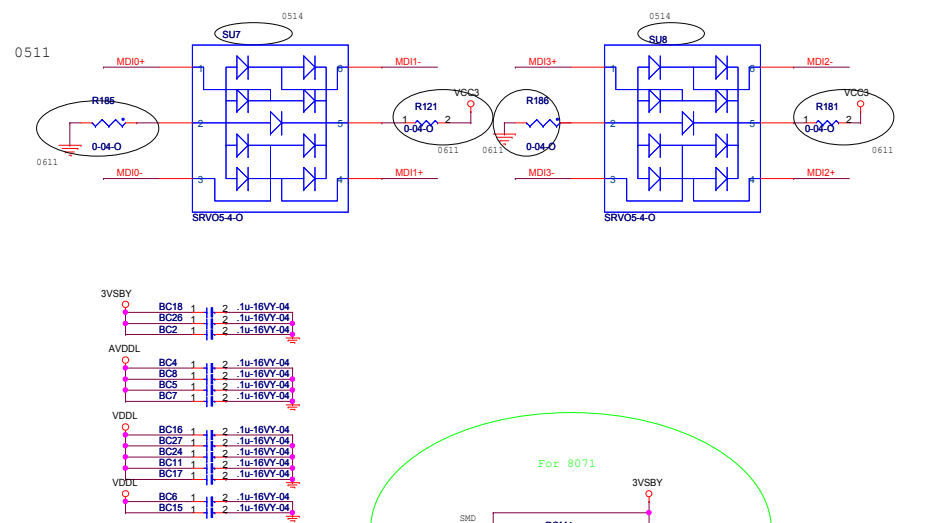
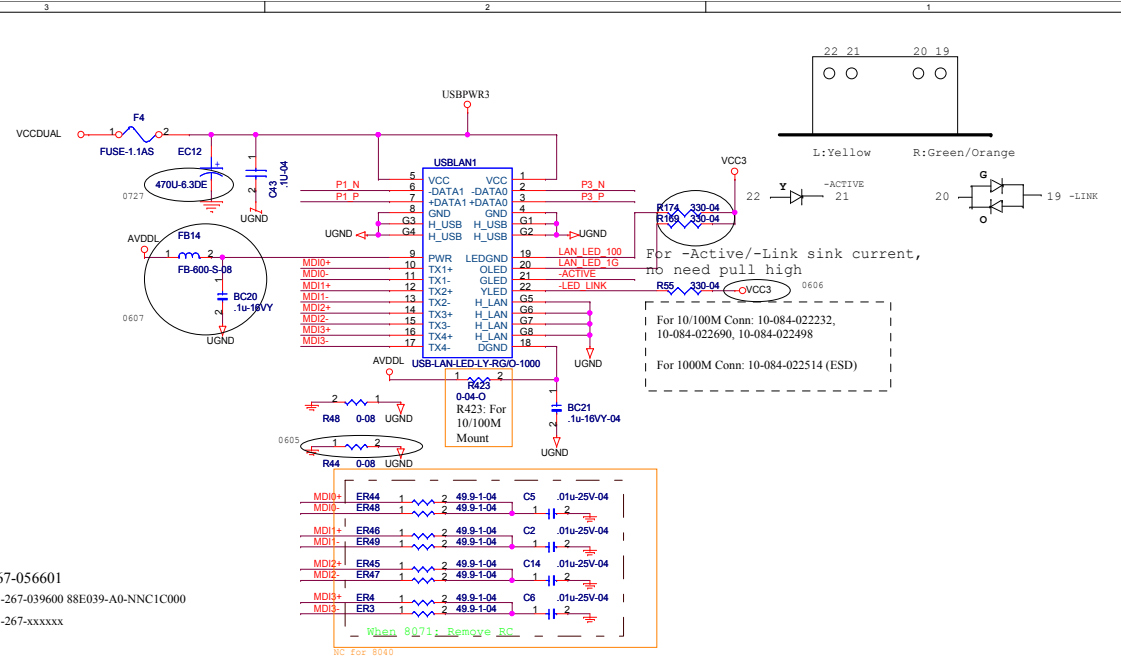


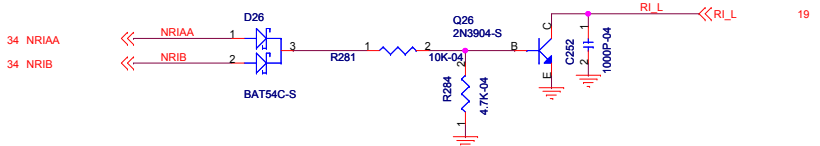
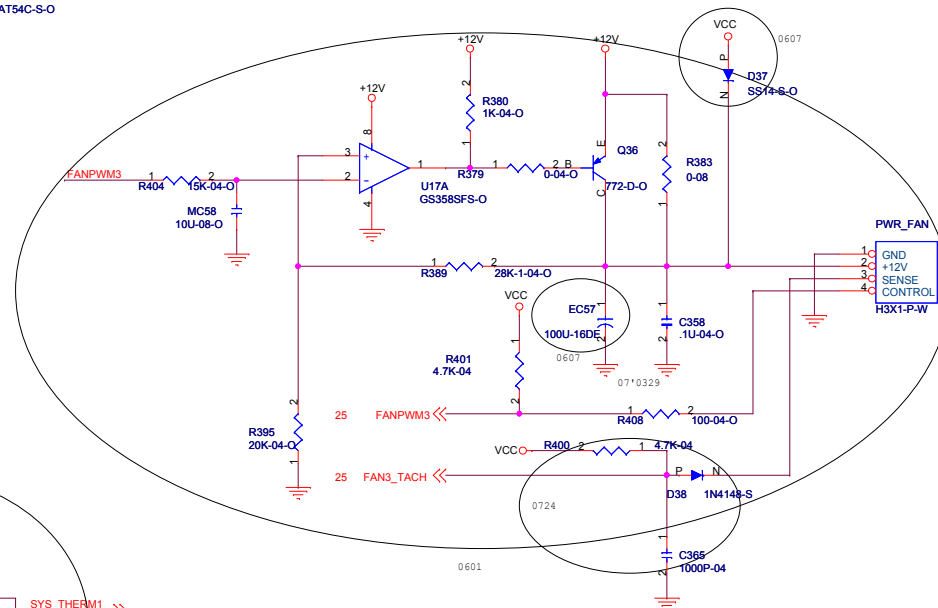
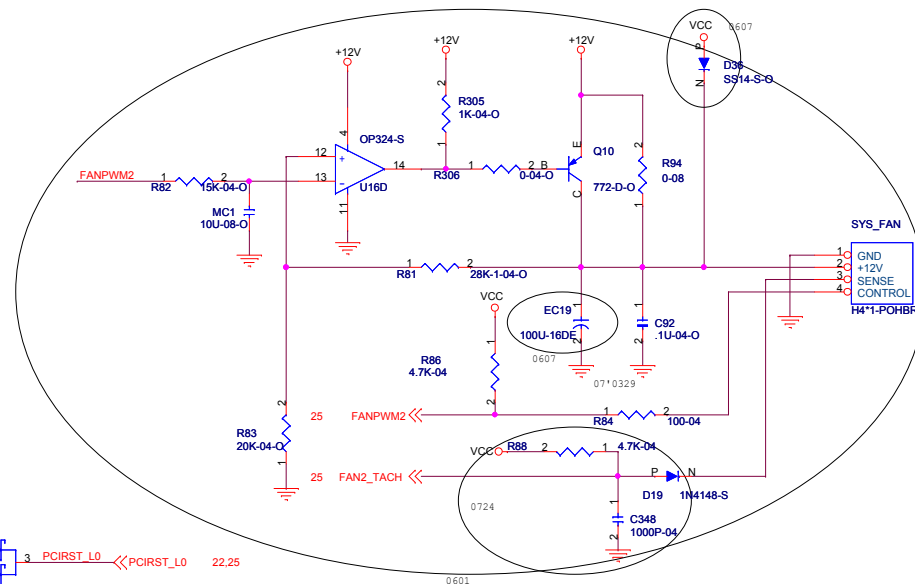
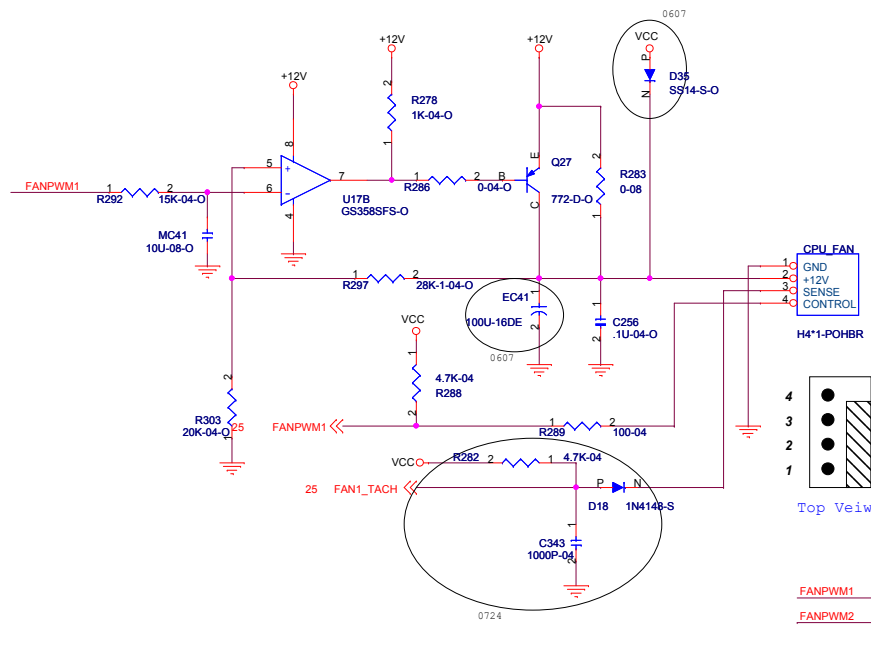




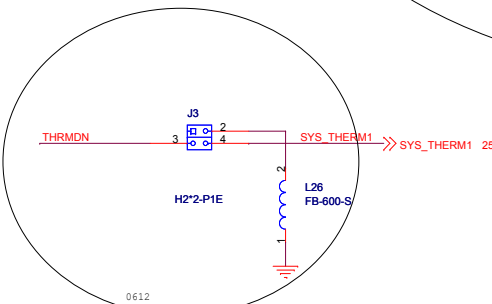
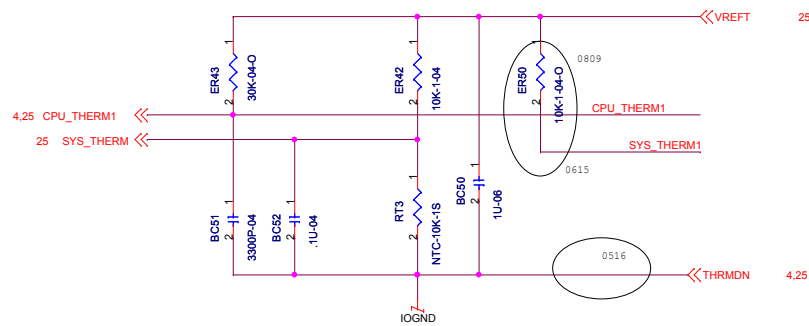


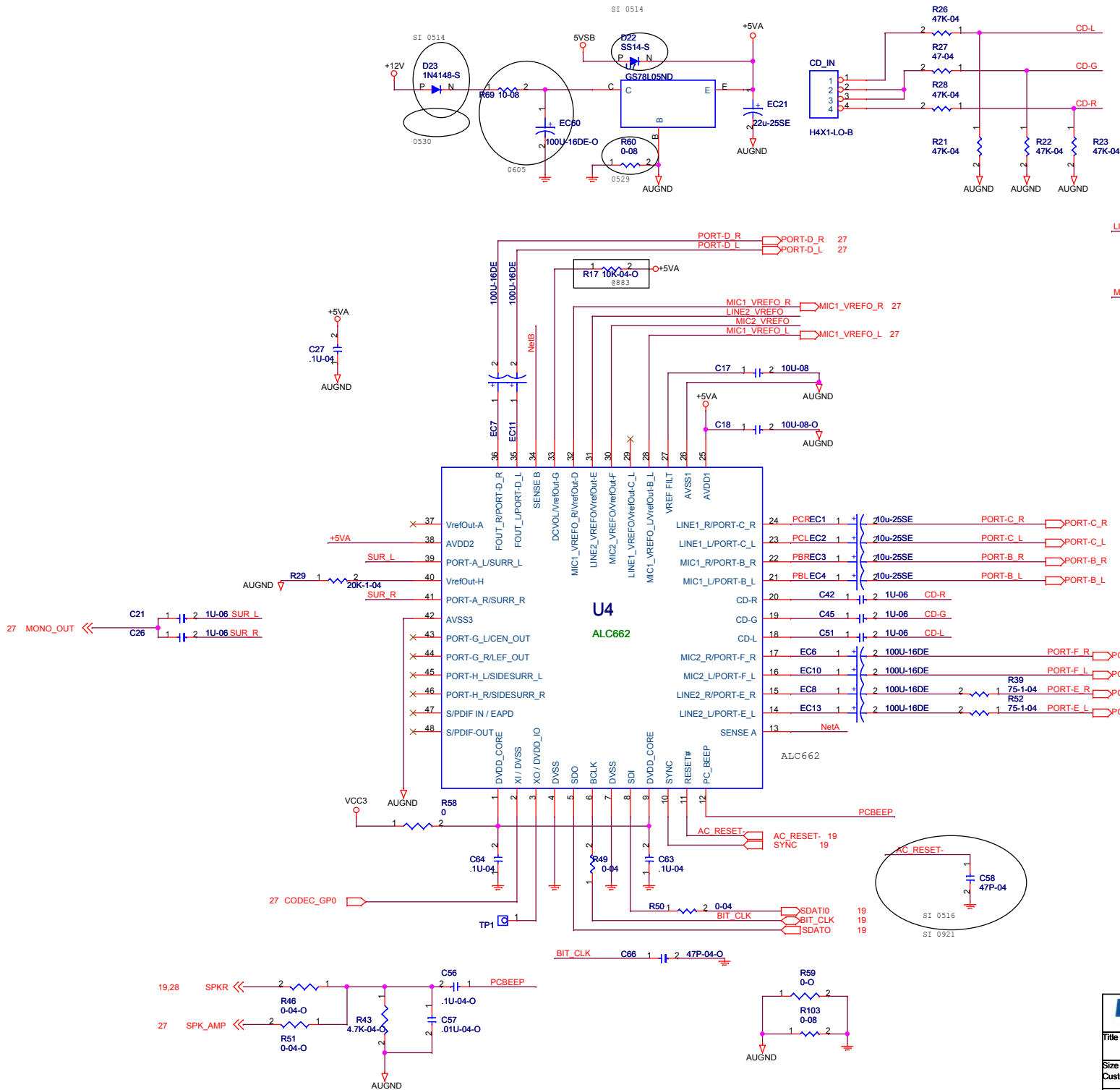




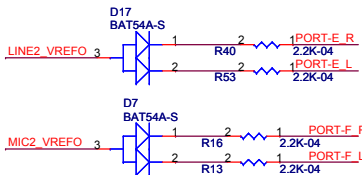


THERM. SENSING



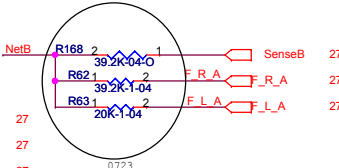
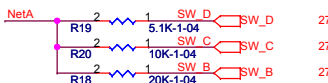


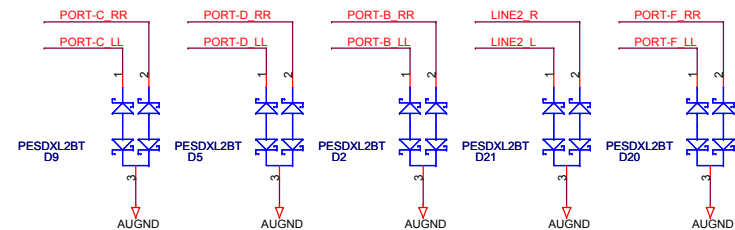
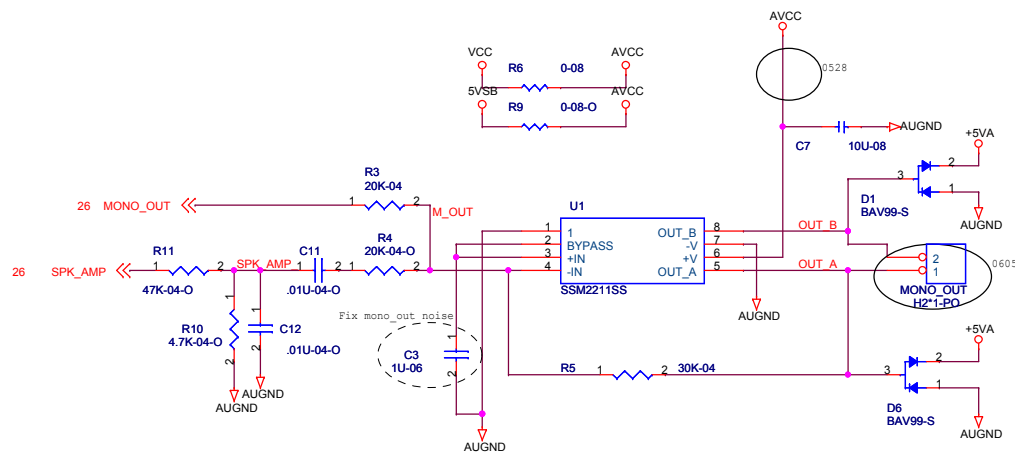
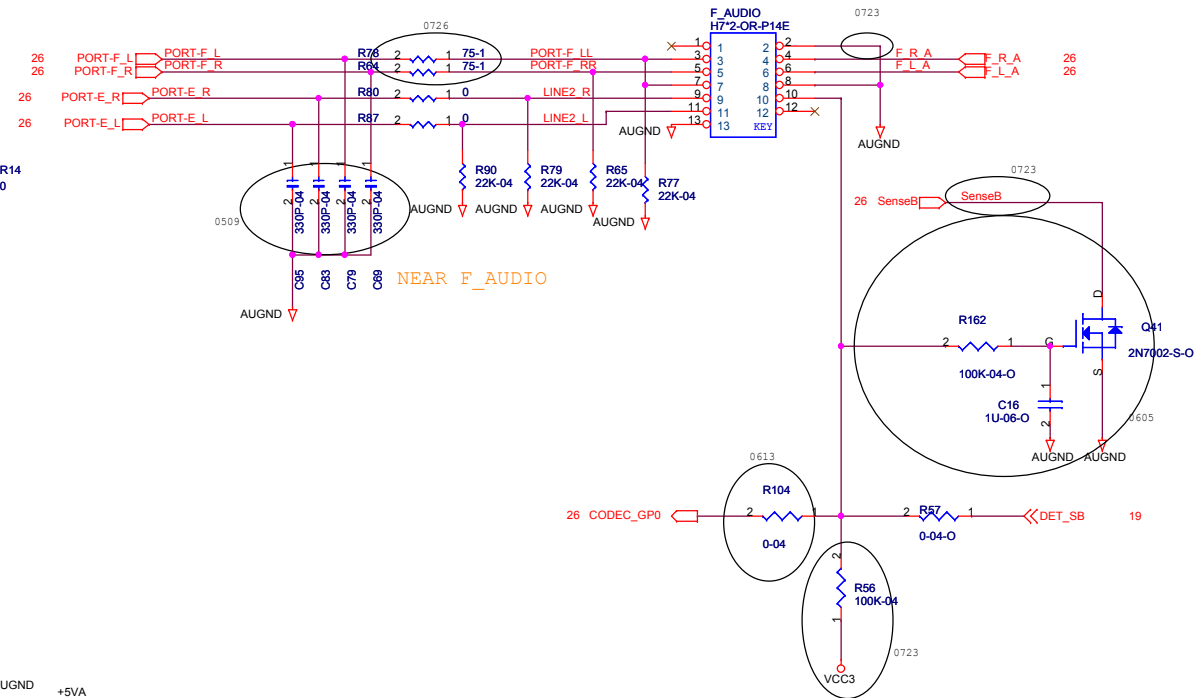
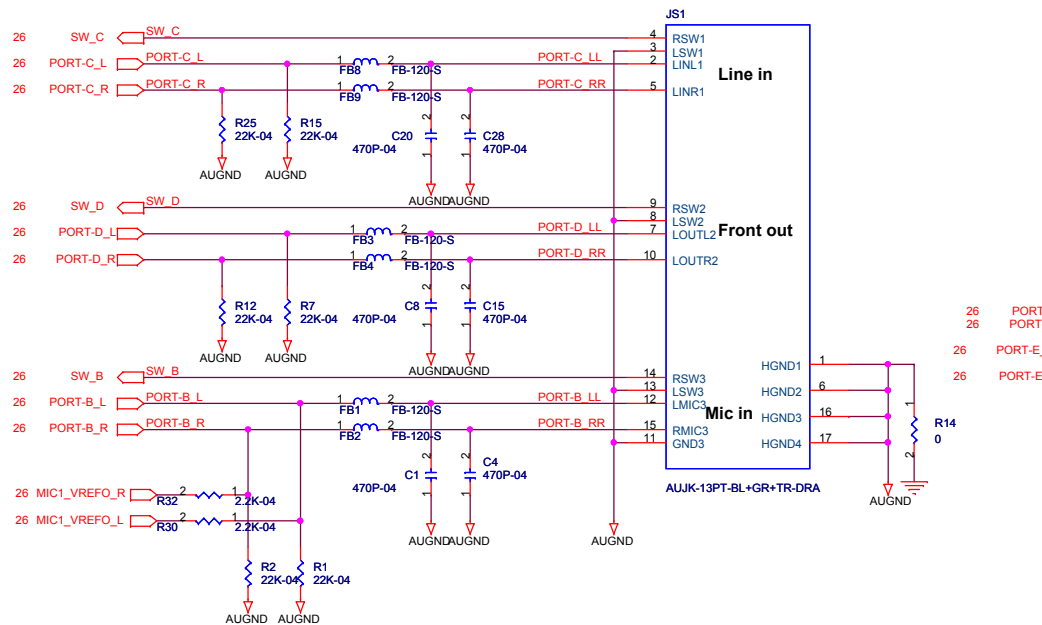
Verfout bias for stereo microphone.



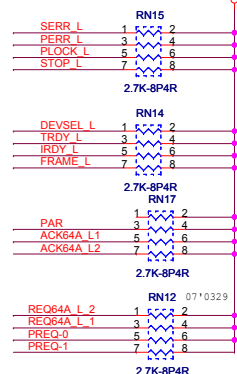
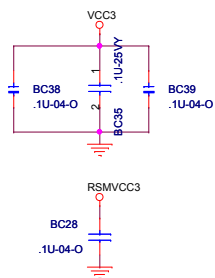
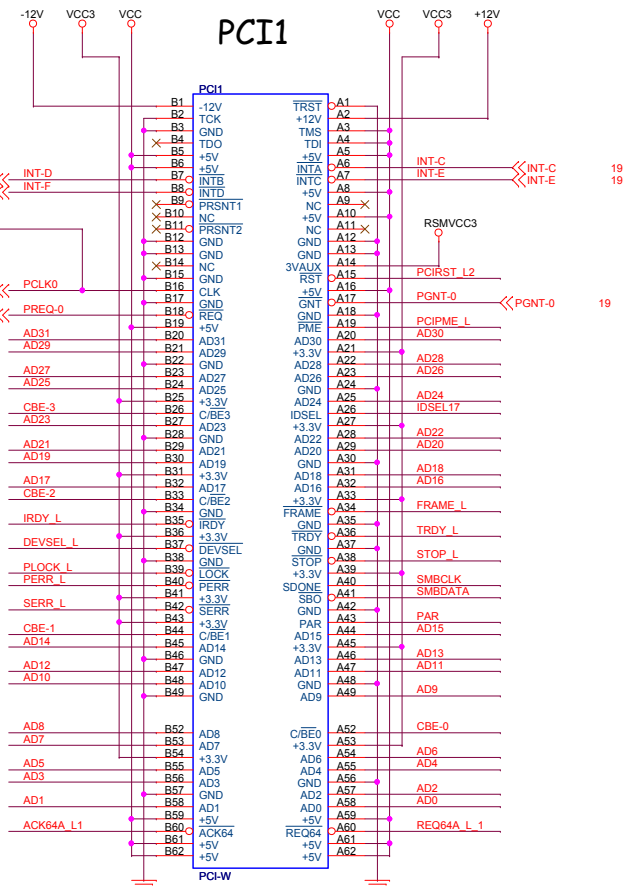
Place near Chip

Resistors Networks

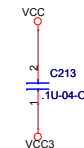
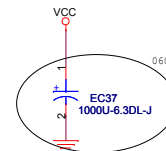
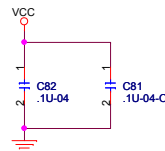




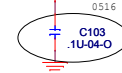
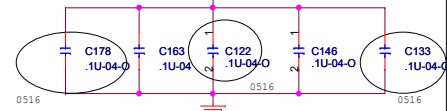
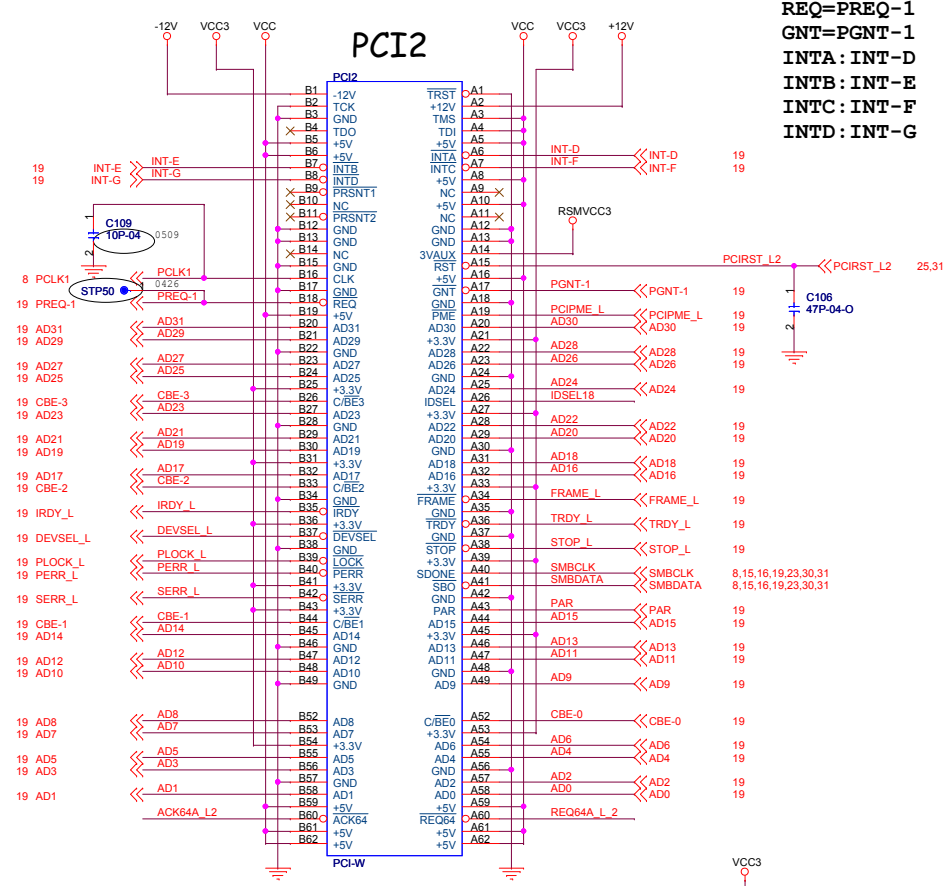
CLK=PCK0
RST=PCIRST_L2
IDSEL=AD17
REQ=PREQ-0
GNT=PGNT-0
INTA: INT-C
INTB: INT-D
INTC: INT-E
INTD: INT-F



NEAR
PCI2
FOR
EMI



PCI2

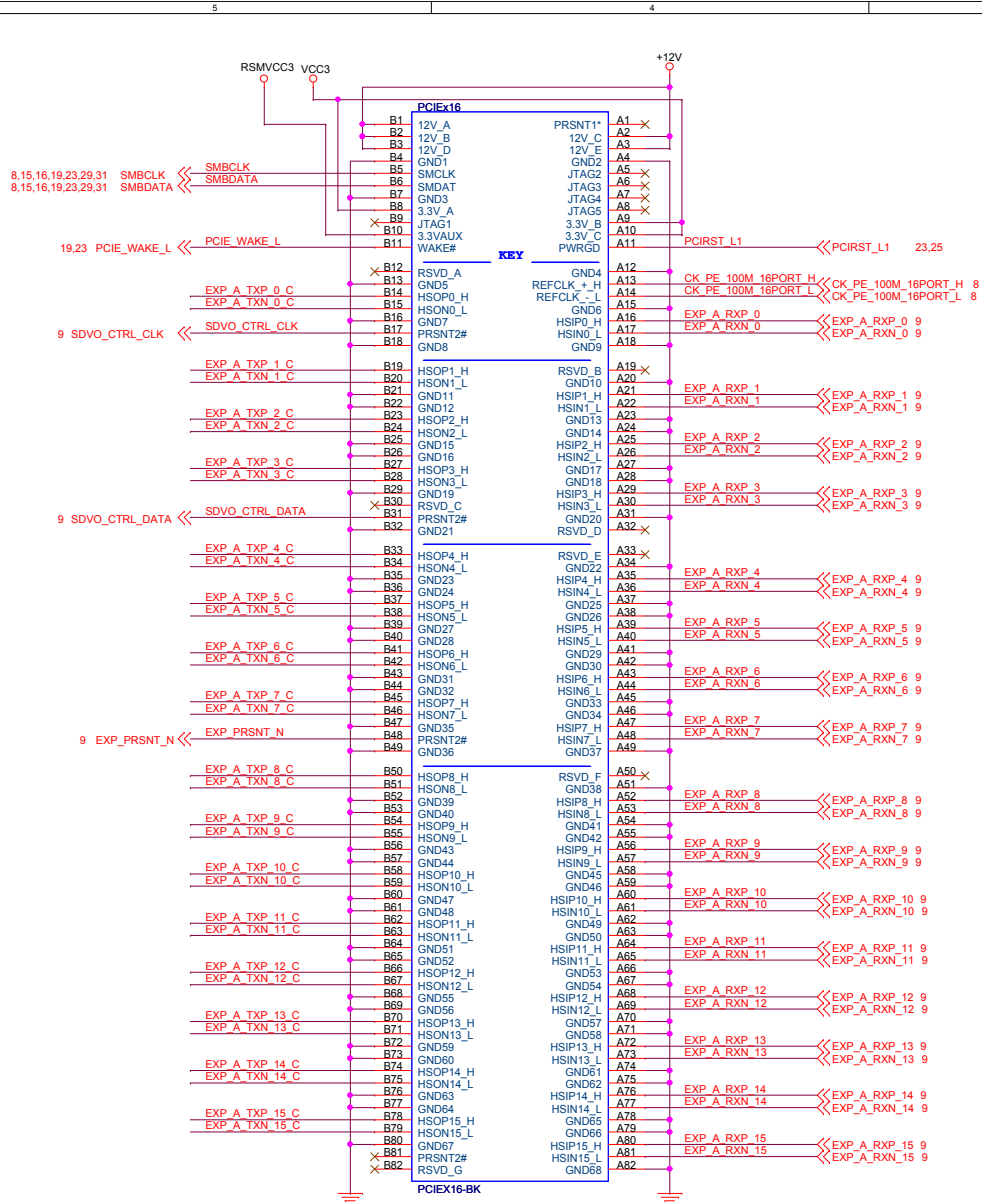


Elitegroup Computer Systems

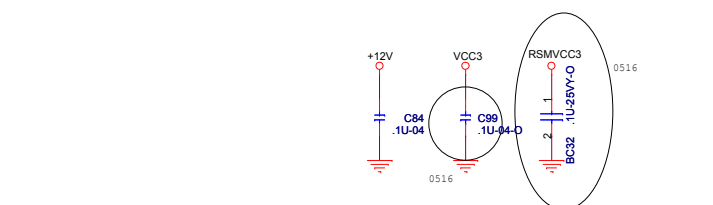
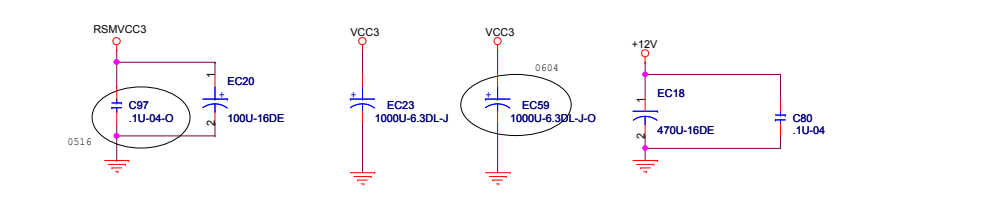
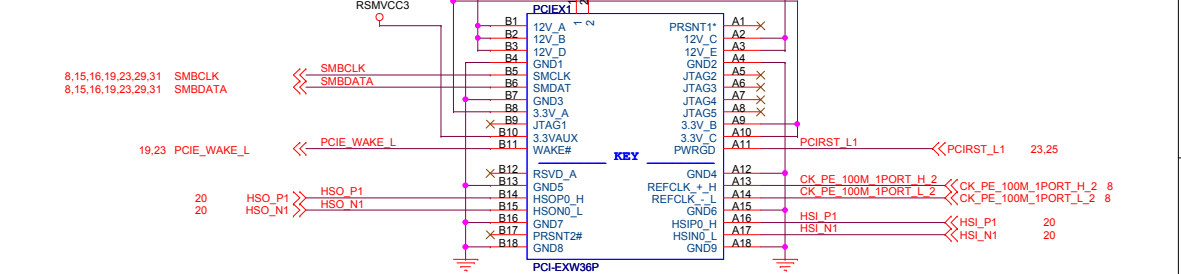
PCI Slot 1&2

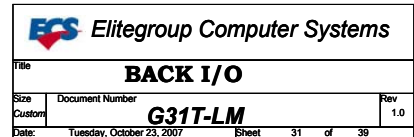
Document Number G31T-LM

Date: Tuesday, October 23, 2007 Sheet 29 of 39

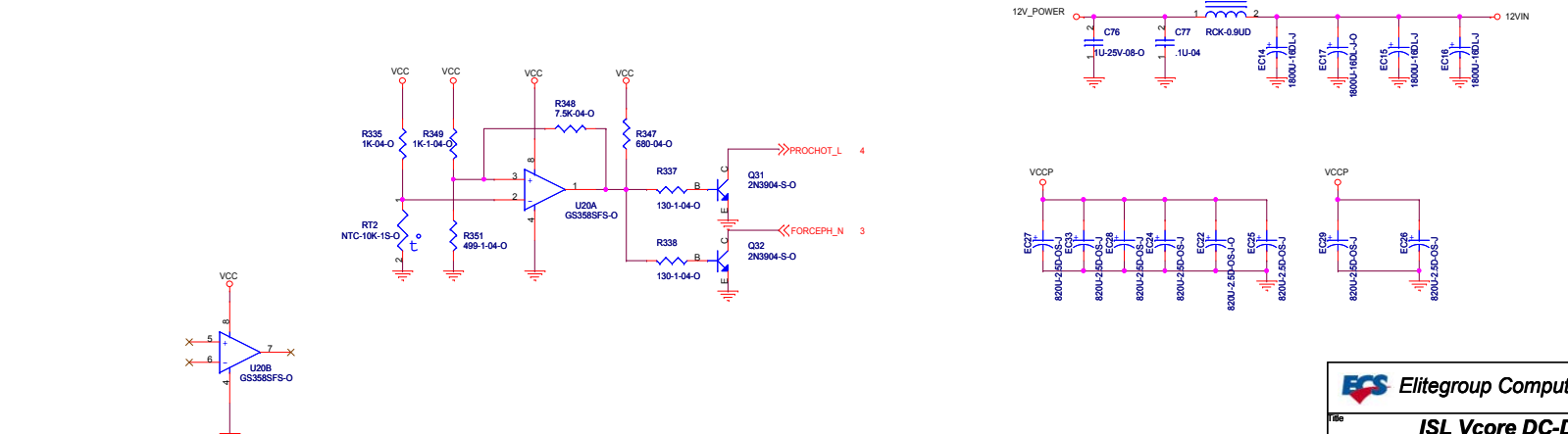
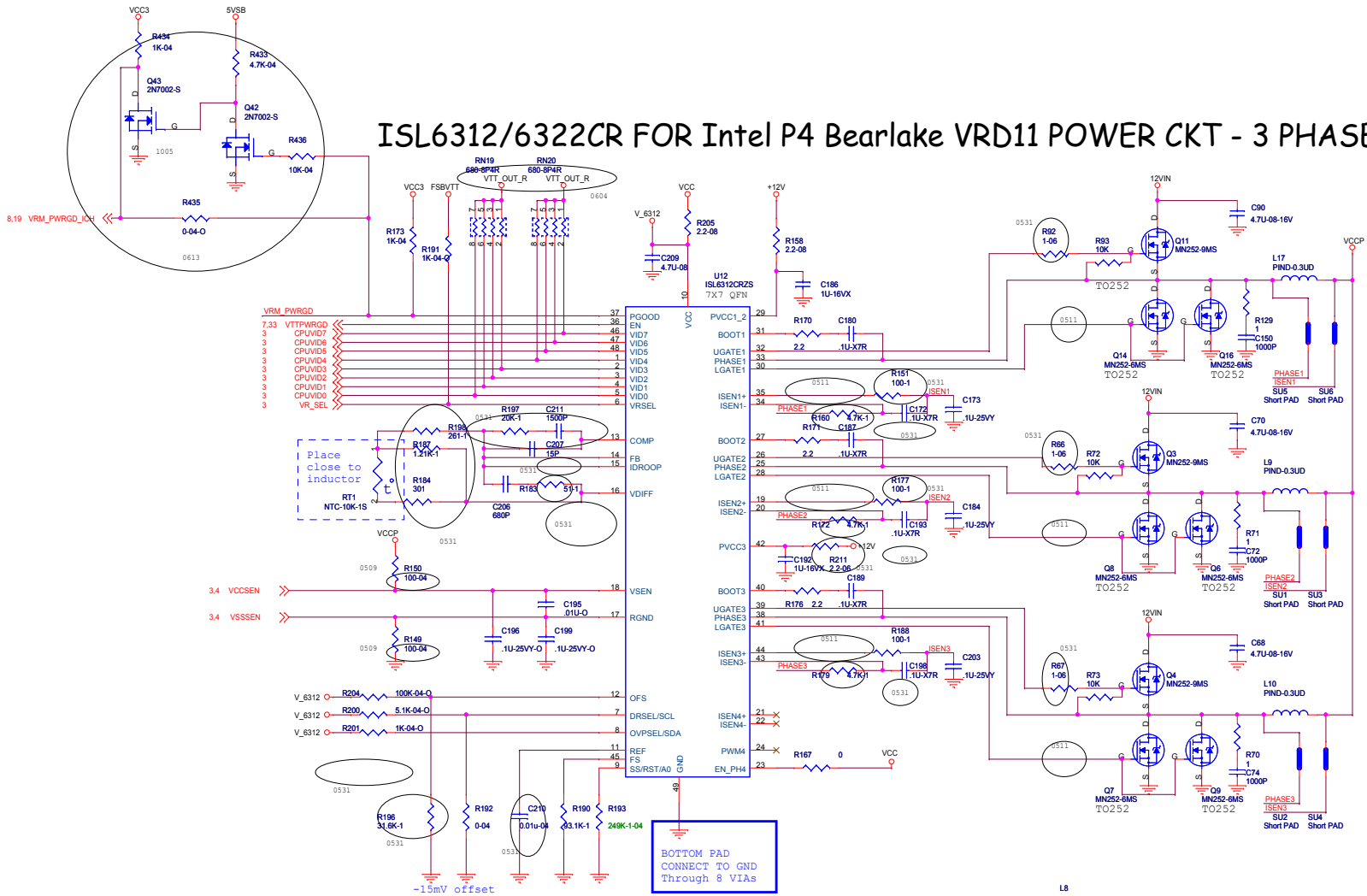


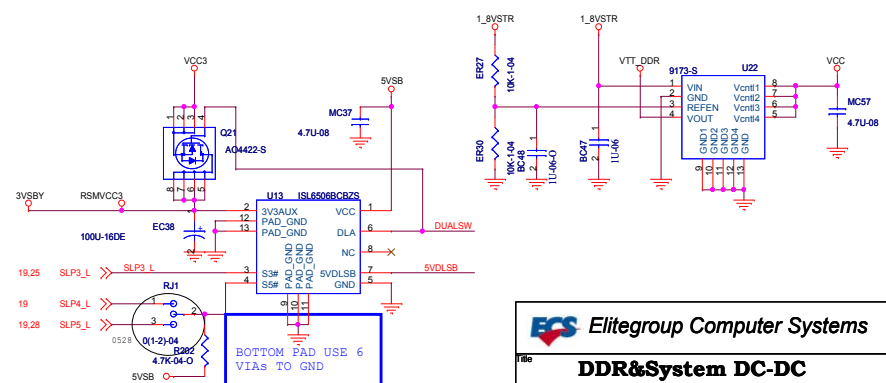
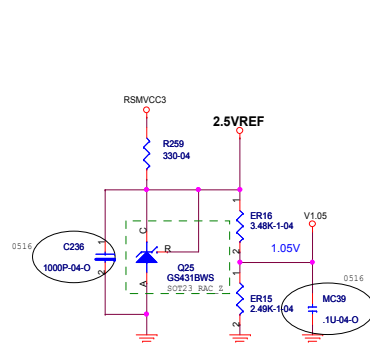
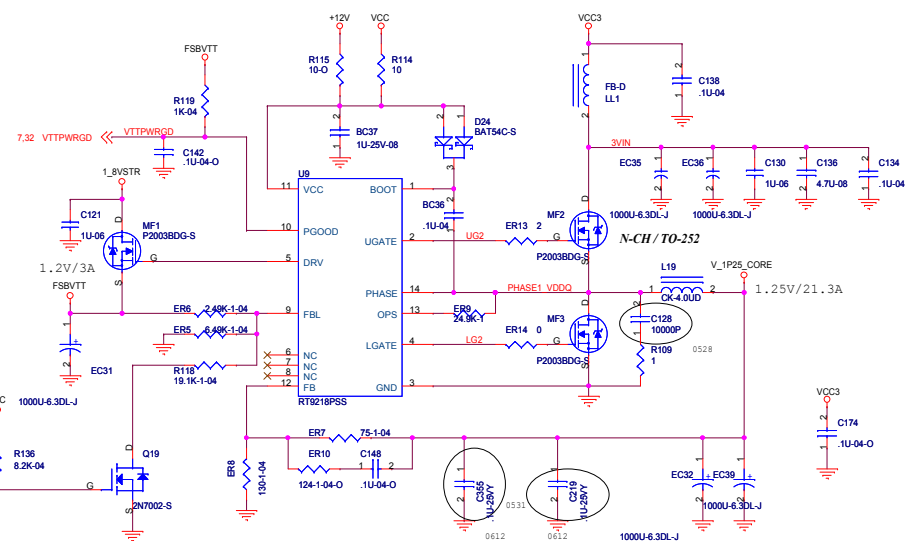
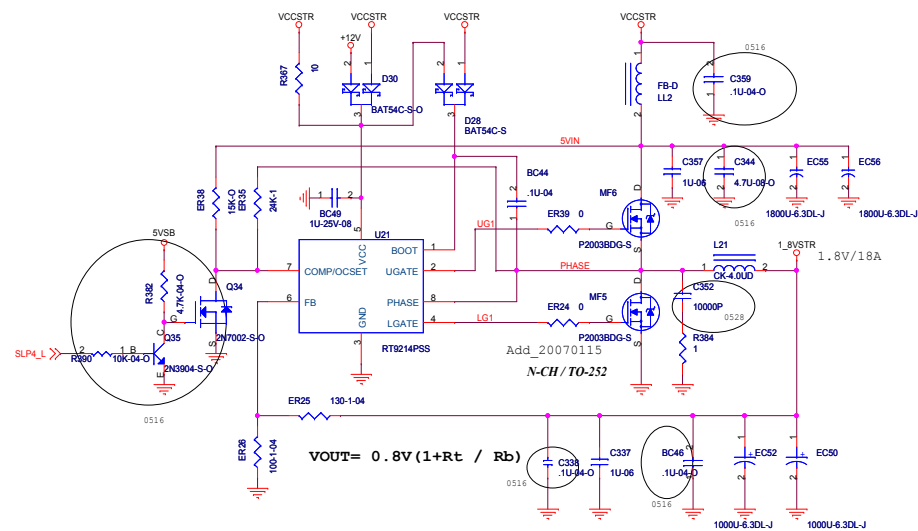
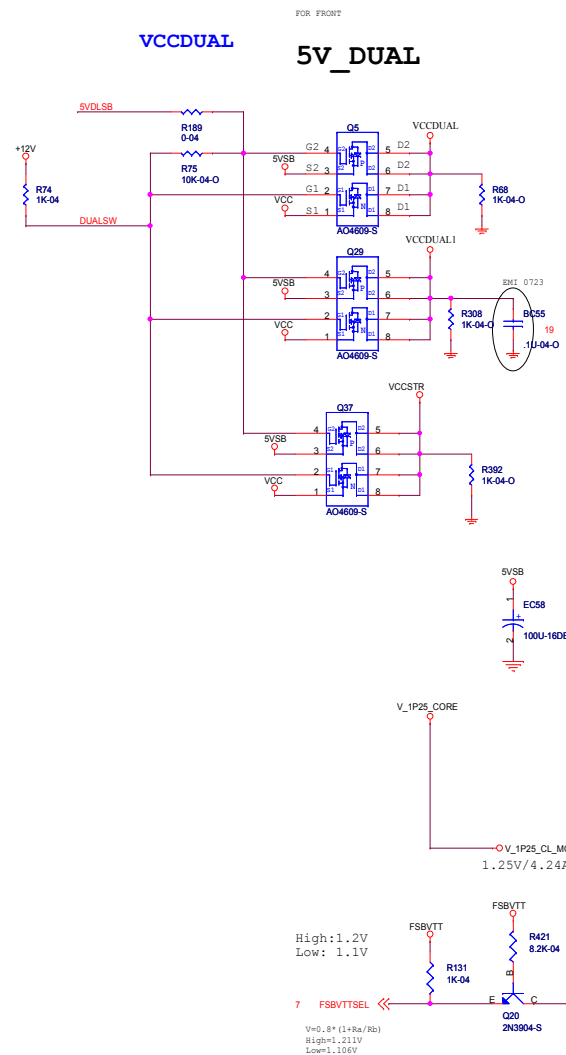
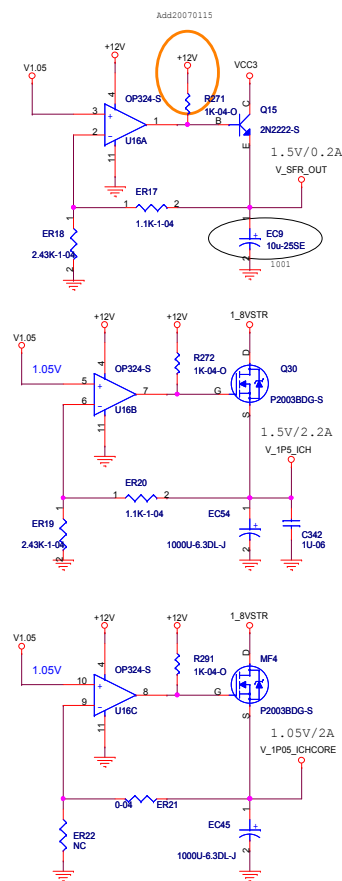
PCI Express SLOT1

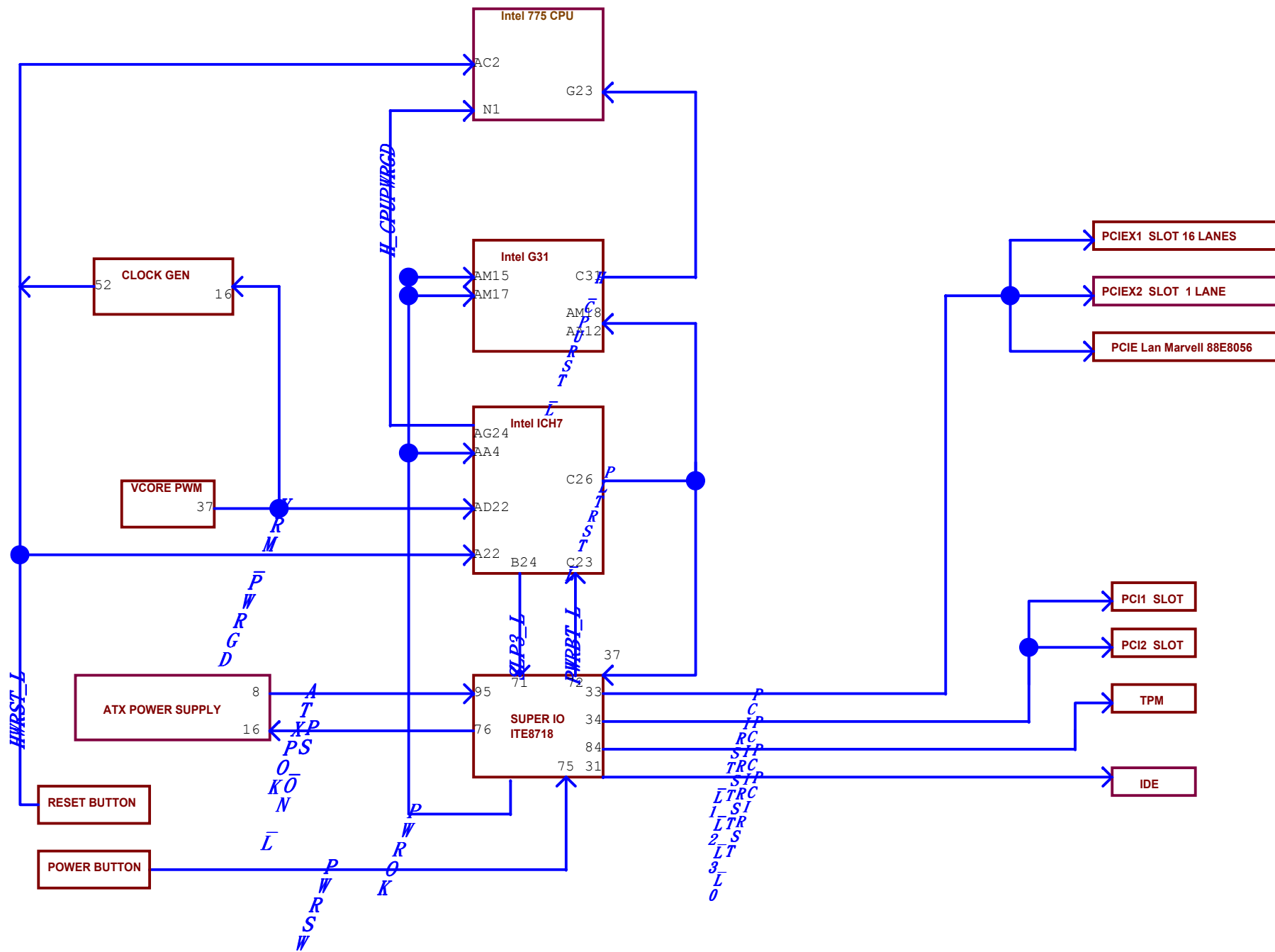


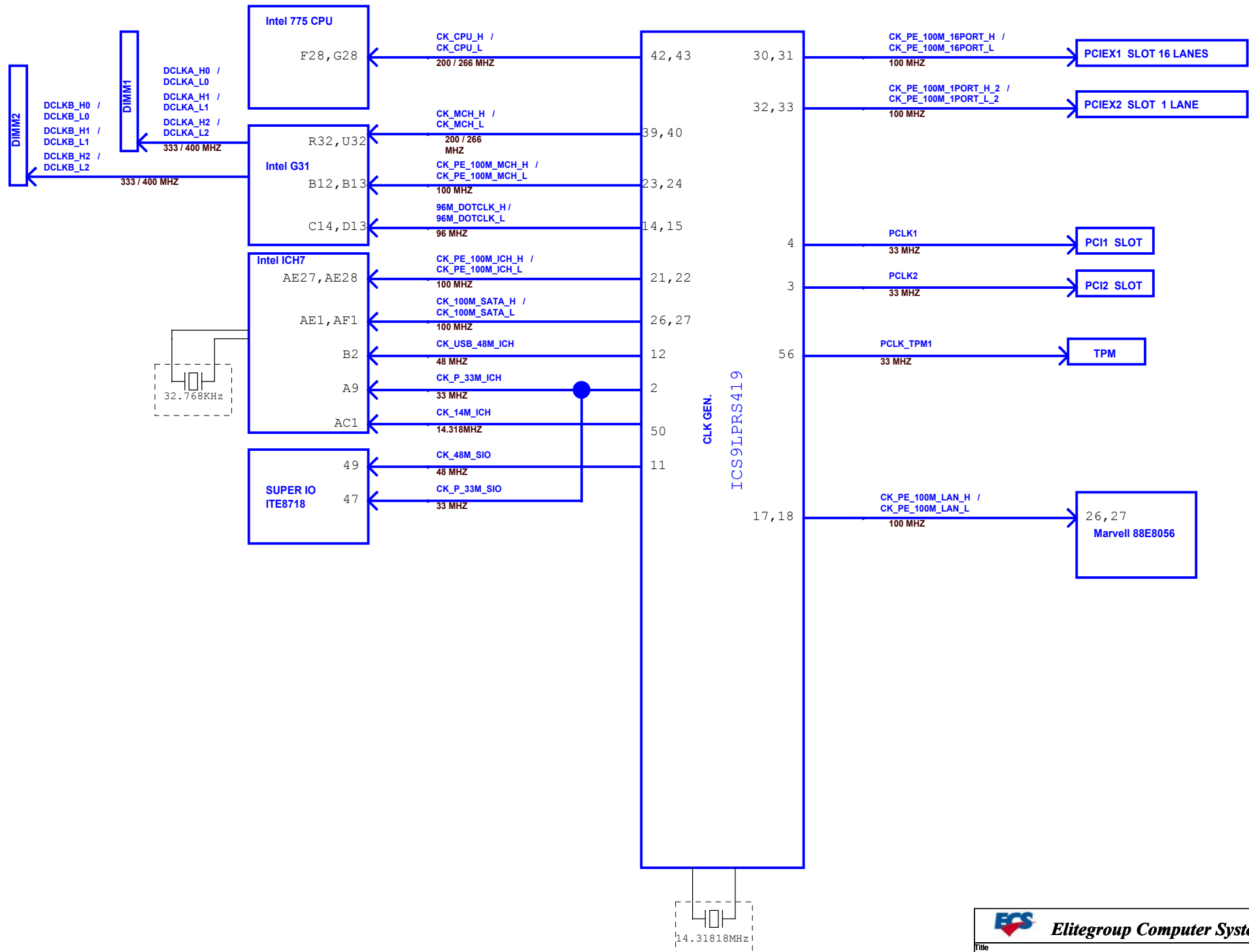


ISL6312/6322CR FOR Intel P4 Bearlake VRD11 POWER CKT - 3 PHASE









ATX4P1	ATX P/S WITH 1A STBY CURRENT					CPU PW
12V +/-5%	5VSB +/-5%	5V +/-5%	3.3V +/-5%	12V +/-5%	-12V +/-5%	12V +/-5%

AO4609

RT9214 SW
POWER1.8V
TO252 * 2

RT9218 SW
POWER1.25V

3.3V LDO
REGULATOR
ISL6506

AO4422

AO4609

5VAA LDO
REGULATOR
78L05

PCI Slot (per slot)	X1 PCIE per	X16 PCIE per
5V 5.0A	3.3V 3.0A	3.3V 3.0A
3.3V 7.6A	12V 0.5A	12V 5.5A
12V 0.5A	3.3Vaux 0.375A	3.3Vaux 0.375A
3.3Vaux 0.375A		
-12V 0.1A		

USB X4 RL	USB X4 RL	2XPS/2
VDD 5VDual 2.0A	VDD 5VDual 2.0A	5VDual 1.0A

INTELSIL 6312

OP_1A
1.2V MOSFET
LINEAR
TO252

OP_2A
1.5V MOSFET
LINEAR
TO252

OP_2B
1.05V MOSFET
LINEAR
TO252

Inte 775 CPU		
VCCP		125A
VTT	1.2V	5.3A

DDR2 DIMMs		
VTT_DDR	0.9V	1A
VDD MEM	1.8V	6A

Intel G31		
VTT	1.2V	1A
VCCSM	1.8V	3.2A
VCC	1.25V	7A
VCC_EXP	1.25V	1A
VCC_CL	1.25V	3.88A
VCCSM	1.8V	3.71A

Intel ICH7		
V_CPU_IO 1.2V	1.2V	14mA
VCC1_5A 1.5V	1.5V	1.01A
VCC1_5B 1.5V	1.5V	0.77A
VCC1_05 1.05V	1.05V	0.86A
VCC3 3.3V	3.3V	0.33A
VCCSUS3_3 3.3V	3.3V	52mA
5VREF 5V	5V	6mA
5V_REF_SUS 5V	5V	10mA
VCCRTC 3.3V	3.3V	TBD uA

ETHERNET		
VDDIO	3.3V	120mA
AVDDL	1.8V	400mA
VDDL	1.2V	200mA

SUPER I/O		
5VSB	5V	
3.3V	3.3V	
BAT 3.3V	3.3V	

AZALIA		
DVDD	3.3V	0.3A
AVDD	5V	0.1A

BATTERY

Schematics Version History Table :

Circuit Ver.	PCB Ver.	Modified Page(s)	Date
B		P3 H_BPM1 disconnect from CPU.C9 pin P8 U8 change to ICS9LPRS419DFLFS P19 Rom table update,R304 8.2K change to 1K,SR10 -O,R302 P20 RJ2(1-2) change to RJ2(2-3) P24 EC57-O Add STP41~ STP51 for ATE test	2007/04/26 -O
		P15 R317 change to 33-04 P12 mount SR1 P19 mount R302 P8 Del Q12,R104 P28 Del Frisw,C355,C349,R374,R375 P34 -O Leo_chip,R175,R180,R209,R207	2007/05/03
		P18 Del Bav99 D3,4,8,10,11,12,13 Add U26,U27 EMI C95,C83,C79,C69=330P U15,U19,U6,U2 chokel,choke2 C33,C25,C263,C274=0.1U remove BC42 C107,C109=10P F7 Add SC45,46,47,48,49,50 -O P3 MC30 change to 0603 P32 R149,R150 change to 0402	2007/05/09
		P18 U26 Vcc3 change to Vcc P23 Add 8111C co-lay P24 mount PWR_FAN	2007/05/10
		1.Del R168,R178,R182,R125,R76,R69 2.Del C181,C190,C202 3.C180,C187,C189,C172,C193,C198 change to X7R 4.LAN chip form RealTek change to Marvell 5.R419 change to 680 Ohm 6.Add C40 for EMI	2007/05/11
		P18 22,C23,C24 change to 4.7P P23 U24,U25 change to SU7,SU8 Add ROM3,ROM4	2007/05/14
		P28 Q33 change to 3904,R373 change to C349 P14 Add C175,C176 P25 Add R424	2007/05/15
		P28 R403,R397 4.7K change to 2k EC34 -O mount C170 C329-O mount C139 C306-O mount C132 C281-O mount C231	2007/05/18
		P20 CLR CMOS value change P25 remove IRDA , add GPIO for MB ID P25 H/W monitor change sensor pin for ITE suggestion	2007/05/24 2007/05/25
		P4 add CPU_GTLREF cap P12 L13,16 change to FB80 P18 remove SR14 P28 mount case open header P33 RJ1 change to (1-2),C352/C128 change to 10000P	2007/05/28
C		P7 CPU top/bottom side Cap modify P32 Vcore power value modify for Intersil FAE suggestion P7 CPU top/bottom side Cap modify P24 Fan control change for Lenovo Spec.	2007/05/30 2007/05/31 2007/06/01 2007/06/01
		P8 Add clk Gen enable signal for Lenovo review P18 Add LC filter for Lenovo review P30 Add EC59 / mount EC37 for Lenovo review P32 VID pull high change to VTT_OUT_R for Lenovo review	2007/06/04
		P18 Add Hsync/Vhsyn Driver for Lenovo review P23 Add 4.7K pull high for Lenovo review P27/P26 modify mono_out/F_panel/ +12V in circuit for Lenovo review	2007/06/05
		P23 Lan LED modify P7 CPU Vcore Cap modify	2007/06/06

Circuit Ver.	PCB Ver.	Modified Page(s)	Date
C		P23 FB14/BC20 footprint change for Lenovo EMI review P24 EC19,EC41,EC57 change for Lenovo review Add D35,D36,D37 for Lenovo review P28 Add Cap for Lenovo review	2007/06/07
		P4 Add test point/TRST# value change for Intel review P8 R91,R97,R95 change 1K for intel review P11 Add SC54 for intel review P12 modify VCCDQ_RTC for intel review P14 Add NB core power CAP for intel review P19 modify net PCIRST L for intel review P21 Add SB power CAP for intel review	2007/06/08
		P4 modify TDO / TRST#.. for intel review P23 ESD power for Lenovo review P12 H_VCCPLL reserve 1.8V for Lenovo review	2007/06/11
		P15 RN39 change to discreate resistor P24,25 Add J3 for Lenovo P33 Add C355 P27 modify R104 P32 VRD_PWRGD modify	2007/06/12 2007/06/13
		V:C change to Ver:0.1	2007/06/13
		P31 remove AT97SC3203 P24 SYS_THERM1 PU to VREF P25 GP30 PU to VCC	2007/06/15
		P25:CHS1 change footprint P31:Add EEP3	2007/07/19
		P19: R428 -Open P8: Add R425 ; CLK modify P23 / P31 : Add C391,C392,C393 for EMI	2007/07/20
		P25:Add RJ8 for ICH case open P27/P26:F_AUDIO modify for Realtek comment	2007/07/23
		P24:Fan tach modify P25:RN53 change to discreate R	2007/07/24
0.1		P23 / P31 EC5,EC12,EC44,EC43 change to 470uF	2007/07/27
		P25 swap CPU & thermal1 net	2007/08/09
		P23 R61 from 0 change to 1K for ATE test	2007/08/14
		P28 Q39,Q40 from 2N3904 change to 2N7002	2007/08/27
		P8 / P32 Add vrm_pwrgrd power sequence P20 ER23 from 20.5 change to 22.6	2007/09/19
		P25 change RSMRST circuit	2007/10/01
0.2		P28 swap F_PANEL power sw	2007/10/23
0.3			
1.0			



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	NC	Mount
INTEL LAN	R298	R299
NO INTEL LAN	R299	R298

	GNT_5	GNT_4
SPI	0	1
PCI	1	0
LPC	1	1

BSEL TABLE				
2 1 0 PSB FREQUENCY				
0 1 0 200 MHZ (800)				
0 0 0 266 MHZ (1066)				

BSEL TABLE				
2	1	0	PSB	FREQUENCY
0	0	0	267	MHz (1067)
0	0	1	133	MHz (533)
0	1	0	200	MHz (800)

FAN_CTL_SEL	
RTSB_L (H) A20GATE_L (L)	11 100%
	10 75%
	01 50%
	00 25%

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Title

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